signal 2′ before switching, now after rearranging the correlators the data bearing signal 3′ will be fed to the demodulator (signal D). The corresponding dashed S curve is shown in Fig. 2*b* where the old equilibrium point R has moved to the right by T_c to form the new equilibrium point R'. After switching, the loop operates again in the linear region of a new S curve. The initial conditions (ICs) of the loop filter must be set by the TSL such that the loop will pass smoothly from the operation before switching to the operation after switching. Of course, some transients cannot be avoided. The switching procedure can be repeated as many times as needed to adapt the individual S curves according to the Doppler effects responsible for the increase or decrease in T/T_c. Only a linear portion of the corresponding individual S curve is ever actually being used for code tracking. Hence, the composite discriminator characteristic is periodic as shown in Fig. 2*b* consisting of straight-line segments from individual S curves. Although the propagation delay time increases or decreases with this switching procedure the relative synchronisation error of the loop $\varepsilon = (\hat{T} - T)/T_c$ with $\hat{T}$ denoting the estimate of T is limited to $|\varepsilon| < 0{\cdot}5$ (modulo operation) and the overall tracking range is a periodic extension of the limited range.

A very important practical case is the tracking loop with $\delta = 0{\cdot}5$. In this case it is possible without adding more complexity to the loop to generate a composite DC which employs hysteresis by choosing the TSL criteria according to $L > 2\,.\,O$ and $E > 2\,.\,O$, respectively [3]. Because the loop operates after switching in the midpoint R of the new S curve we obtain a composite DC that consists of overlapping linear portions of the individual S curves. This is in contrast to Fig. 2*b* where the linear regions are non-overlapping. In fact it will be important to avoid the assignments of the code positions being switched back and forth under noisy conditions as will be encountered in cases with sawtooth characteristics as in Fig. 2*b*, for example.

It is obvious that the TDL and the double-dither loop [2] can be easily extended by the ACTL concept because they themselves are modified versions of the DLL. The MCTL [1] has an S curve consisting of segments of parabolas. By applying appropriate criteria to the TSL a new MCTL with a periodic composite discriminator characteristic having again segments of parabolas and also with hysteresis will result. In the encountered examples full-wave rectifiers were used as envelope detectors. Of course, square-law detectors can be used as well. In such cases the criteria given in Table 1 have to be adapted to the corresponding shape of the squared ACFs.

Comparison with DLL: A brief comparison based on computer simulations between the DLL and the ACTL in a noiseless environment for $\delta = 0{\cdot}5$ and for a code length of 31 is shown in Fig. 3 where both loops were of first order. Fig. 3*a* shows that the DLL can track a large constant Doppler shift due to a relative constant velocity between the transmitter and receiver only for a short time. After this time the DLL loses lock because the resulting loop steady state error does not exist (i.e. is not within the limited range of the S curve). Hence, the DLL has no chance to re-lock by itself. The ACTL instead is able to track the same Doppler shift by switching the correlator arms accordingly (Fig. 3*b*).

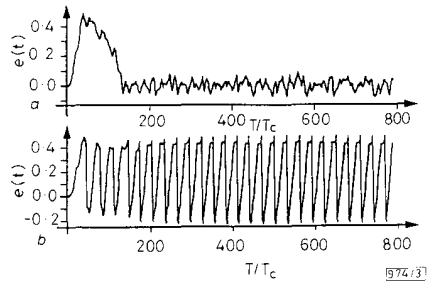

Fig. 3 *Loop error signal of DLL and ACTL subject to constant Doppler shift*
a DLL
b ACTL

Conclusions: By using the ACTL with three correlator arms shifted relative to each other it is possible to track a PN code subject to Doppler effects. Owing to the periodic discriminator characteristic these effects are taken care of by an adaption of the arms whereas the channel noise can be suppressed by a narrower loop compared to the classical DLL. Of course, the ACTL can also lose lock because of some improper switching behaviour due to high channel noise. This can be improved by employing switching criteria resulting in a periodic discriminator characteristic with hysteresis. Also, because the three arms are identical, they can all be used in the code acquisition phase in order to speed up this process by a factor of three.

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LOW THRESHOLD VOLTAGE VERTICAL CAVITY SURFACE-EMITTING LASER

K. L. Lear, S. A. Chalmers and K. P. Killeen

Indexing terms: Lasers, Semiconductor lasers

Vertical-cavity surface emitting laser diodes with threshold voltages as low as 1·48 V are demonstrated. The devices have low-resistance epitaxial mirrors, and current passes through the entire mirror stack. The low threshold voltage results from both low threshold current densities and mirrors with low resistivities even at low current densities. The laser fabrication sequence is relatively quick and simple and allows for the rapid characterisation of vertical-cavity surface-emitting laser material.

Vertical cavity surface emitting lasers (VCSELs) have developed rapidly during the past few years, but their performance is still hampered by high mirror resistances due to large potential barriers at each heterojunction in the mirror stacks. Previously, high threshold voltages, typically 3 V or more, were symptomatic of these high parasitic series resistances which also caused poor efficiencies and other problems associated with excessive heating [1]. Recently, alternative laser structures have been developed in which the current flow bypasses the top mirror giving threshold voltages as low as 1·7 V [2]. We report a VCSEL threhold voltage of 1·48 V in an all-epitaxial semiconductor structure in which current flows through the entire mirror stack. The reduction in threshold voltage results from greatly reduced mirror voltage drops due to low resistivity mirrors with completely linear current–voltage characteristics [3] and low threshold current densities due to an efficient cavity design and high reflectivity mirrors. Highly conducting VCSEL mirrors are necessary for the planar, implant isolated fabrication approach [4], but also could be used to advantage even in lateral injection approaches.

Our all-epitaxial structure was grown by molecular-beam epitaxy and included low resistivity Be-doped and Si-doped AlGaAs mirrors. The mirror interfaces are continuously graded from 10 to 90% AlAs mode fraction by varying both the aluminium and gallium effusion cell temperatures using a method similar to that reported previously [5]. We adjusted the temperature profiles to give an eight-segment piecewise linear approximation to a sinusoid, and obtained linear current–voltage characteristics with resistivities as low as $1{\cdot}8 \times 10^{-5}\,\Omega\,cm^2$ for 20 period mirror stacks with Be doping concentrations of $5 \times 10^{18}/cm^3$ [3]. The importance of current–voltage linearity is manifest in the characteristics of a typical superlattice graded mirror and the continuously graded mirror shown in Fig. 1. Although these two alternate grading schemes can produce roughly similar differential resistivities at high current densities, the voltage drop of the 8 segment mirror is much smaller at low current densities ($< 500\,A/cm^2$). Threshold current densities in this range are achieved in this work and have been reported by other groups [6, 7]; they are expected to become typical for high performance VCSELs.

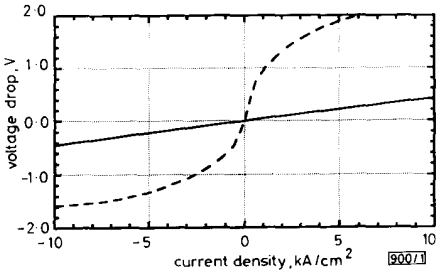

Fig. 1 *Voltage against current density for 20 period mirror stacks with 8 segment/period compared with superlattice graded mirror*

The voltage drop is that measured for the mirror stack alone; contact and substrate voltage drops have been subtracted
——— 20 period mirror stacks (8 segment/period)
– – – – superlattice graded mirror

We have combined our mirrors with a triple InGaAs quantum well cavity to produce a very low threshold voltage VCSEL structure. The growth begins with 35 periods of an Si doped mirror on an *n*-type substrate following which the majority of the cavity is grown. The growth is then interrupted to measure the reflectivity spectrum. Based on the measured wavelength of the cavity mode and mirror stop band, the layer thicknesses for the remainder of the cavity and the 22 period Be-doped mirrors are adjusted to correct the cavity and mirror centre wavelengths [8]. This single measurement ensures a highly accurate cavity wavelength that typically falls within 0·25% of the desired value.

To assess the VCSEL design and material quality, bottom-emitting devices of various sizes were fabricated from this epitaxial structure. Devices were made with a single photolithographic step which defined an evaporated pure gold circular or square contact by liftoff. In addition to functioning as electrical contacts, the gold features enhance the reflectivity of the top mirror and serve as masks for a phosphoric wet etch used to isolate devices. The etch went part way into the lower mirror stack as well as undercutting the gold contact by $\sim 3\,\mu m$ at the junction plane. A blanket Ge/Au/Ni/Au *n*-type contact was then evaporated on the sample. The overhanging perimeter of the gold contact formed by the wet etch undercut prevented the *n*-type contact metal from landing on the sloped mesa side and shorting out the junction.

The devices were driven CW, and the power emitted through the polished but uncoated substrate was measured with a calibrated silicon photodiode. All current–voltage measurements were verified to within 1 mV using multiple instruments. The light–current and voltage–current characteristics of a diode with a $25\,\mu m$ diameter junction are presented in Fig. 2. The device exhibits a 2·9 mA, 1·48 V lasing threshold which is only 0·23 V in excess of the photon energy corresponding to the lasing wavelength of 990 nm. Neighbouring devices had similar characteristics. The ripple in the output power curve is a result of the coupling with the cavity formed by the bottom mirror and the uncoated substrate. Despite the high bottom reflectivity and the substrate reflection, the output power peaked at 0·6 mW. Measurements on larger devices with a $42 \times 42\,\mu m^2$ square junction gave CW threshold currents as low as 8·1 mA or threshold current densities of $460\,A/cm^2$. These large devices produced 2·5 mW of output power at 60 mA and lased to currents greater than 100 mA.

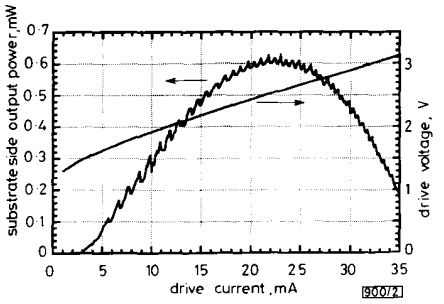

Fig. 2 *Light and voltage against current characteristics for 25 μm diameter mesa etched VCSEL*

The measured power output is consistent with that expected from a simple calculation of external slope efficiency using estimates for mirror reflectivities, internal quantum efficiency, and free carrier absorption, but neglecting other losses such as scattering and diffraction. The bottom mirror of the VCSEL structure has 35 periods with a calculated reflectivity of 99·86%. The top mirror is 21 periods ending in a $\lambda/4$ layer that in combination with the semiconductor–air interface gives a reflectivity of 99·27%. This design is ultimately intended to be used for top emitting devices with the top output coupler transmissivity being much greater than that of the bottom high reflector. However, the addition of gold on the top mirror boosts the calculated reflectivity of the top mirror to 99·87%. Note that the reflectivity is increased by the gold even in the absence of an additional $\lambda/6$ phase matching layer that would have maximised the reflectivity [9]. The estimated round trip free-carrier absorption is 1% which, being much larger than the mirror losses, dominates the total losses and leads to poor slope efficiencies. By dividing the bottom mirror transmissivity by the total losses and assuming an 80% internal quantum efficiency and further accounting for the 30% reflection at the uncoated substrate to air interface, we estimate an external slope efficiency of 6%. This calculated value agrees well with the measured value for the large devices.

The fabrication sequence described here offers a convenient means for the rapid fabrication of VCSELs to evaluate epitaxial structure design and quality. It is not, however, intended to give optimum laser performance. The high mirror reflectivities lower the threshold but greatly diminish the power output. The low mirror loss emphasises the effect of other loss mechanisms such as free-carrier absorption, diffraction, and scattering. The conical shape of the lasers not only contributes to diffraction losses but accentuates the contact and upper mirror resistance because their areas are smaller than the junction area. The importance of reducing the contact and other parasitic resistances along with that of the *p*-type mirror is evident from examining the total series resistance of our lasers. The slope of the current–voltage curve in Fig. 2 gives a differential resistance of 45 Ω above 15 mA. This is 10 times higher than the resistance expected due to the approximately $2 \times 10^{-5}\,\Omega\,cm^2$ *p*-mirror contribution. Hence, the other parasitic resistances are now dominant and must be reduced for further device improvement.

In summary, we believe we have demonstrated a record low CW threshold voltage for VCSELs. This low voltage results from a low threshold current density of $460\,A/cm^2$ in combination with a mirror having low resistance at these current densities. The devices have been fabricated by a method which allows for quick evaluation of InGaAs quantum well VCSEL material including that designed for top emitting structures.

More optimum fabrication approaches using this epitaxial structure and attention to other parasitic resistances should result in yet better performance.

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EXTRACTION OF PHYSICAL DEVICE DIMENSIONS OF SOI MOSFETs FROM GATE CAPACITANCE MEASUREMENTS

D. Flandre and B. Gentinne

Indexing terms: MOSFETs, Capacitance measurement, Silicon-on-insulator structures and devices

A new technique unique to SOI MOSFETs is presented for extracting the physical device dimensions (effective gate length and gate oxide and film thicknesses) from a set of gate capacitance measurements on transistors with various lengths. In this Letter, the technique is extended to the simultaneous extraction of the effective gate length and of the gate oxide and film thicknesses from a set of gate capacitance measurements on transistors with various lengths. Subsequently, the technique is also validated for the extraction of the film thickness on devices with short dimensions.

Introduction: Gate capacitance measurement of MOS transistors is widely used for the characterisation of bulk Si devices [1]. In SOI technology, such measurements have seldom been reported [2–6] and the use of the method has so far has been restricted to the extraction of the SOI film thickness from measurements on very large devices [4–6].

Limitations of previous technique: The technique presented in Reference 4 to extract the film thickness T_{soi} of an SOI MOSFET was based on the variation of the capacitance measured between gate and source/drain with front-gate (V_{gs}) and back-gate voltages (V_{bs}) [2, 3]. At low V_{bs}, the capacitance curve of an SOI MOSFET is quite similar to that of a conventional bulk MOSFET (Fig. 1): in the cutoff regime, a minimum value C_1 corresponding to the parasitic and gate-overlap capacitances is observed, whereas in the turn-on regime, a maximum value C_0 close to the total oxide capacitance C_{ox} is obtained. At high positive V_{bs}, the cutoff curve changes dramatically: a value C_2 is observed which is much larger than C_1. This has been related to the formation of an inversion layer at the film/buried oxide interface, so that C_2 can be associated with the series combination of the fully-depleted film capacitance ($C_{soi} = W \cdot L \cdot \varepsilon_{si}/T_{soi}$) and of the total oxide capacitance. From this intuitive interpretation, the following formula was derived in Reference 4:

$$T_{soi} = W \cdot L \cdot \varepsilon_{si} \cdot \frac{C_0 - C_2}{(C_0 - C_1) \cdot (C_2 - C_1)} \quad (1)$$

This formula was initially developed for very large devices (W and $L > 50\,\mu m$). To extend its validity to devices with more practical dimensions, it is not sufficient to account for the effective gate length L_{eff} and width W_{eff}. Inaccuracies in the measurement of the capacitance values should be adequately assessed.

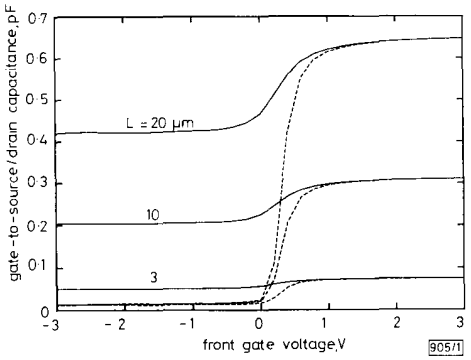

Fig. 1 *Gate capacitance measurements on SOI n-MOSFETs with different lengths for near-zero and very positive back-gate voltages*
$W \simeq 50\,\mu m$, $T_{ox} \simeq 52\,nm$, $T_{soi} \simeq 90\,nm$
– – – – near-zero back-gate voltage
——— very positive back-gate voltage

On one hand, appropriate shielding and a careful calibration procedure are used to eliminate the stray capacitance due to the connection leads to the device under test. An incomplete elimination however does not affect our calculations, because the stray component can be assumed constant throughout the measurements and all the extraction formulas are based on differences of capacitance values.

On the other hand, fringing capacitance effects may not be totally neglected. C_1 indeed incorporates inner (C_{if}) and outer fringing (C_{of}) capacitances, related to the existence of electric field line between gate and source/drain either inside or outside the device active area. Whereas the outer fringing is almost bias-independent and is hence removed by capacitance subtraction, the inner fringing value strongly depends on the applied biases [7]. It is maximum for C_1, but completely vanishes for conditions corresponding to the measurement of C_0 due to the shielding effect of the front inversion layer. Regarding C_2 because there is no front inversion, we will assume this