NMOS Device Characteristics in Electron-Beam-Recrystallized SOI

Lance R. Thompson, *Member, IEEE*, James R. Buser, *Member, IEEE*, Jack D. Meyer, *Member, IEEE*, Cameron A. Moore, *Member, IEEE*, Jay T. Fukumoto, *Member, IEEE*, and George J. Collins, *Fellow, IEEE*

***Abstract*—Characteristics of n-channel MOSFET's fabricated in cold cathode electron-beam-recrystallized silicon-on-oxide layers have been examined. Assorted crystallographic defects exist in the recrystallized silicon layer ranging from highly branched subgrain boundaries to widely spaced parallel subgrains and rows of threading dislocations. Some of these MOSFET transistors have characteristics approaching those fabricated in bulk silicon including $\approx$ 828-cm^2/V · s electron surface mobilities and 130-mV/decade inverse subthreshold slopes. However, many of the devices tested exhibited leakage currents up to 10^{-6} A/μm, resulting in high inverse subthreshold slopes and reduced threshold voltages. Some effects of crystal imperfections on device behavior are discussed.**

I. Introduction

SILICON-ON-INSULATOR (SOI) films provide the possibility of producing MOSFET circuits with increased speed, latch-up immunity, improved radiation hardness, and three-dimensional circuitry [1], while retaining the benefits of highly developed bulk silicon processing. Recently, optical waveguides [2] that are vertically integrated [3] have also been achieved using SOI. Each of the leading SOI techniques, such as Separation by the IMplantation of OXygen (SIMOX) and Zone Melt Recrystallization (ZMR), have had their own set of materials limitations. SIMOX layers, for instance, have been plagued by metal impurities, oxide precipitates, and a high density of defects at the SOI/isolation oxide interface. In addition, SIMOX wafers are expensive due to the high-power oxygen implanter employed requiring a major capital equipment upgrade to scale with each increase in wafer diameter. Alternatively, the ZMR technique produces SOI films by employing manufacturing equipment of significantly lower cost. However, ZMR SOI material is plagued by high densities of crystalline defects which form grain and subgrain boundaries. Progress in the elimination of these defects during the ZMR process has been made in the last few years including reduction of subgrain boundary branching, increased subgrain boundary spacing, and reduction in defect density within the subgrain boundaries. Research into the elimination of these defects and analysis of their effect on transistor characteristics is still ongoing.

We have been investigating a cold cathode line-source electron beam as the heat source in a ZMR technique for achieving SOI films [4], [5]. The cold-cathode electron gun utilized has the ability to generate a high current (0.7 A), low voltage (1 to 5 kV) [6], narrow width (approximately 2 mm full width at one half maximum) electron beam [7], which can be easily scaled in length to greater than 20 cm. The cold-cathode electron beam requires only soft vacuum (0.5 torr) for operation, unlike hot-filament electron sources previously investigated for ZMR where high vacuum ($< 10^{-6}$ torr) systems are required [8]. Thus the scalability and the operating conditions of the cold-cathode electron-beam source may allow the production of SOI wafers at a low cost.

The crystallographic quality [9] and electrical transport properties [10] of electron-beam ZMR SOI material have been examined previously. Herein, we discuss characteristics of enhancement-type n-channel MOSFET's fabricated in electron-beam-recrystallized SOI material. The best transistors examined exhibit values of majority-carrier surface mobility, inverse subthreshold slope, and leakage current comparable to those for bulk silicon n-channel MOSFET's. However, the present transistor performance characteristics, especially the off-state leakage current, vary from device to device across a typical electron-beam-recrystallized SOI wafer and as yet do not meet VLSI device requirements.

II. Recrystallization Conditions

The SOI wafers examined here are created with 10-cm-diameter, (100)-oriented, 650-μm-thick, 1- to 10-Ω · cm, electronic-grade silicon wafers as the substrate. Each SOI

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L. R. Thompson is with Storage Technology Corporation, Louisville, CO 80028-5219.

J. R. Buser is at Hewlett-Packard, Colorado Integrated Circuits Division, Fort Collins, CO 80525.

J. D. Meyer and G. J. Collins are with the Department of Electrical Engineering, Colorado State University, Fort Collins, CO 80523.

C. A. Moore is with the Department of Engineering, University of Denver, Denver, CO 80208.

J. T. Fukumoto is with NCR Microelectronics, Fort Collins, CO 80525.

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wafer has a starting structure consisting of a 2-μm-thick thermally grown SiO_2 isolation layer and a 1-μm-thick overlayer of LPCVD polysilicon. A 1-μm SOI layer thickness is employed here because of the difficulty in recrystallizing thinner films with our present experimental apparatus, presumably due to the increased thermal gradient induced in thinner films. Control of the lateral thermal gradient has been shown to be a critical parameter determining the resulting crystalline quality of a recrystallized SOI layer [9]. Although a thinner SOI layer would insure device isolation while enhancing performance by accessing the fully depleted mode and would be a goal of further studies, these 1-μm films are useful to provide data on the SOI layers' electronic properties.

Carbon is implanted into the overlying polysilicon film with a dose of 10^{15} cm^{-2} at 75 keV to act as a wetting agent during electron-beam ZMR. Following the implant, we deposit a 2-μm-thick LPCVD SiO_2 film to act as an encapsulation layer [11]. Both the carbon implant and the encapsulation layer prevent the silicon film from agglomerating during recrystallization. A secondary ion mass spectroscopy depth profile taken after recrystallization indicates impurity concentrations of carbon at 5×10^{18} cm^{-3} and oxygen at 4×10^{19} cm^{-3} exist throughout the SOI layer.

The wafer is oriented on a substrate heater/translation stage with its primary [110] flat at a 45° angle with respect to the linear electron beam in order to reduce wafer warpage during recrystallization. An array of tungsten halogen lamps raises the background temperature of the wafer to approximately 1250°C prior to ZMR. The starting wafer is then recrystallized in a single pass under the 14-cm-long line-source electron beam at a scan rate of 0.5 mm/s. Although seeding of the overlying Si layer to the underlying single-crystal (100)-oriented Si substrate is not employed, the resulting recrystallized SOI layer has predominately a (100) texture as observed previously [9], [12]. Following ZMR, the wafers are typically macroscopically warped with a deviation of up to 100 μm across the wafer diameter due to thermal stress induced by nonuniform heating during the ZMR process (this warpage has been reduced to less than 50 μm for subsequent device fabrication by backlapping the wafer). The warpage could be further decreased in the future by increasing the uniformity of the background and linear heat sources and by reducing thermal gradients by variation in ZMR process parameters. Thus small-geometry lithography which is precluded by the present extent of warpage may be realized in the future. Slight deviations in the thermal gradient at the trailing edge of the molten zone thermally induces stress in the solidifying silicon which is relieved by the formation of subgrain boundaries consisting of densely packed line defects. These subgrain boundaries disrupt the single-crystal nature of the film as they run nearly parallel to the recrystallization scan direction with 30- to 100-μm spacings and vary in type across the wafer from chevron branched boundaries (with planar deviations of $\leq 1°$) to rows of discontinuous boundaries (consisting of arrays of discrete threading dislocations with planar deviations $\leq 0.2°$ and spacing parallel to the boundary of 1 μm). We have previously reported these phenomena for SOI films produced by electron-beam ZMR [5], [8], [9] as have others for other ZMR techniques [12], [13]. It is uncertain how these subgrain boundaries will affect the electrical transport properties of these SOI layers. It has been suggested that subgrain boundaries present a potential barrier to carrier transport resulting in higher resistance perpendicular to the boundary relative to that in a parallel direction [14]. Additionally, a given residual stress has shown to enhance transport of one carrier type and to decrease that of the other carrier type, although this is a negligible effect for the stresses found in ZMR SOI films when the substrate is silicon [15].

III. Device Processing

Hewlett-Packard's Instrument Division (Loveland, CO) processed the electron-beam ZMR SOI wafers as part of a bulk silicon commercial lot. The transistor characteristics presented below come from 12 test pattern areas on these wafers. Each test strip contained 8 n-channel MOSFET transistors with width–length (W/L) aspect ratios of 40/40, 40/5, 40/4, 40/3, 20/4, 5/20, 4/40, and 5/40, where all these dimensions are in micrometers. The source and drain regions of the NMOS devices are heavily doped n-type, while the channel is doped p-type with 2.2×10^{11} cm^{-2} boron ions at 75 keV. The gate dielectric is 750 Å of thermally grown SiO_2 and the gate interconnect is deposited polysilicon. The field oxide extends nearly but not completely through the SOI layer leaving approximately 1000 Å of silicon under the field oxide. All process steps during the fabrication of the NMOSFET's are exactly those used in the processing of bulk Si, that is, no special precautions or added steps have been incorporated to optimize the process for the SOI wafers. A depiction of the devices in this test strip is shown in Fig. 1.

SOI material recrystallized under similar electron-beam ZMR conditions has been characterized previously by Hall effect and four-point resistivity measurements at room temperature to be n-type with less than 10^{12} carriers/cm^3 with 10^4 Ω · cm bulk resistivity. For low-temperature Hall measurements, the ZMR SOI film was implanted with 10^{12} phosphorus ions/cm^2 at 60 keV and subsequently annealed to achieve a uniform doping of 10^{16} atoms/cm^3 through the SOI layer. The room-temperature Hall mobility of majority carriers (electrons) for the phosphorus-doped films was measured to be 900 cm^2/V · s which is approximately two-thirds that of bulk Si for a similar doping density [10].

IV. Transistor Characteristics

Initial characterization of the SOI NMOS transistors include measurements of I_{ds} (V_{ds}, V_{gs}) characteristics, where the body of the SOI film is left floating, the source electrode is set to 0 V, and I_{ds}, V_{ds}, and V_{gs} are measured as shown in Fig. 1 using an HP4145 semiconductor param-

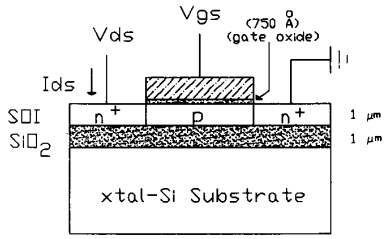

Fig. 1. NMOS ZMR SOI transistor.

eter analyzer connected to a probe station located in a light-tight box. The body of the SOI film in each of these measurements is left floating. Parameters extracted from these scans include the off-state drain-to-source leakage current (I_L), the threshold voltage (V_t), the effective electron surface carrier mobility (μ_n), and the inverse subthreshold slope (S). The value of V_t is evaluated experimentally via (1) and theoretically calculated via (2), while μ_n is evaluated experimentally via (3).

$$I_{ds} = (\mu_n C_i W/2L)(V_{gs} - V_t)^2 \text{ (A)} \quad \text{(Experimental)} \tag{1}$$

$$V_t = 2|\phi_p| + qQ_s/C_i + (2\epsilon_s qN_a 2|\phi_p|)^{1/2}/C_i \text{ (V)} \quad \text{(Theoretical)} \tag{2}$$

$$\mu_n = (\Delta I_{ds}/\Delta V_{gs})\frac{L}{WC_iV_{ds}} \text{ (cm}^2\text{/V} \cdot \text{s)} \tag{3}$$

where ϵ_s is the permittivity of silicon, N_a is the doping density of the channel, ϕ_p is the Fermi potential, C_i is the gate–insulator capacitance, and Q_s is a collective term containing any interface-trap densities of fixed oxide charges. The values of S and I_L are extracted directly from the parametric data as discussed below. In addition, characteristics of the n^+-p junctions (drain-to-body and source-to-body junctions) have been examined under both forward and reverse bias to determine the origin of the excessively high leakage currents found in many of the devices.

I_{ds} versus V_{ds} curves for a typical electron-beam-recrystallized SOI NMOS transistor are shown in Fig. 2, where V_{gs} is increased from 0 to 4 V in 1-V steps. Note that the SOI layer is not fully depleted, as indicated by the characteristic kink in the I_{ds}–V_{ds} curves. The kink is associated with the floating-body effect which is common for non-fully depleted SOI MOSFET's [16]. Although it has been observed that the kink can be eliminated, and the inverse subthreshold slope can be decreased in fully depleted SOI transistors [17], no attempt was made to thin the 1-μm SOI layer during the NMOS device fabrication.

The intercept on the V_{gs} axis of a straight-line tangent to the steepest linear region of an $I_{ds}^{1/2}$ versus V_{gs} plot, where V_{ds} is set equal to V_{gs} throughout the measurement range, is used to experimentally determine the threshold voltage V_t of the devices according to (1) [18]. The threshold voltage (V_t = 1.2 V) found experimentally from

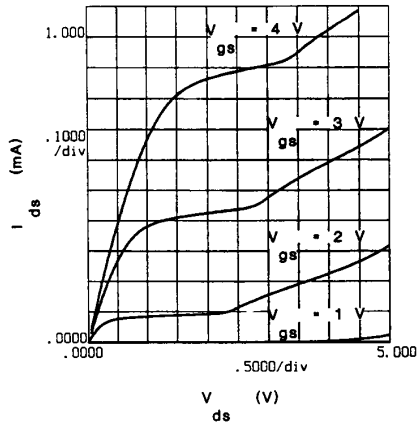

Fig. 2. I_{ds} versus V_{ds} curves for a typical electron-beam-recrystallized SOI NMOS transistor, where V_{gs} is increased from 0 to 4 V in 1-V steps, W = 40 μm, L = 3 μm.

the intercept in this way for the device of Fig. 2 compares well to the theoretical value of 1.1 V calculated according to (2) with Q_s equal to zero. A value for Q_s of -1.8×10^{10} cm^{-2} in (2), typical for this process line, adjusts the theoretical value of V_t to the experimental one (the intercept value). The channel doping density used to calculate the Fermi level in these calculations is 9.7×10^{15} cm^{-3} as estimated from the dose (2.2×10^{11} cm^{-2}) divided by the projected range (0.225 μm) expected from implantation of boron ions into Si at 75 keV.

Plots of I_{ds} versus V_{gs} with V_{ds} = 1, 3, and 5 V for the device whose I_{ds}–V_{ds} characteristics are given in Fig. 2 are found in Fig. 3. The inverse subthreshold slope (S) of the device is determined to be 130 mV/decade from the reciprocal of the slope of the curves in Fig. 3 as labeled. The magnitude of the off-stage leakage current, also obtained from Fig. 3 with V_{gs} = 0 V and V_{ds} = 1 V, was 1 pA which is at the noise limit of our measurement apparatus. The off-state leakage current remains constant for increasingly negative values of V_{gs} but rises with increasing V_{ds}.

A significant number of the devices tested have higher off-state leakage currents than the device of Figs. 2 and 3. The leakage current for these devices is determined by the value of the current I_{ds} flowing at V_{gs} = 0 V and V_{ds} = 1 V as shown in Fig. 3. Fig. 4 displays the number of devices for all devices probed exhibiting leakage current normalized to W at each order of magnitude ranging from 10^{-14} to 10^{-5} A/μm. The devices with high leakage currents also exhibit degraded performance in terms of increased inverse subthreshold slopes and reduced V_t values as shown in Figs. 5 and 6, respectively. When the devices are more and more nonideal (due to high leakage currents) the calculations of V_t, S, and μ_n tend to lose their meaning but Figs. 5 and 6 do depict at what magnitude of leakage current and to what extent these devices become nonideal. Fig. 5 plots the inverse subthreshold slope versus the normalized leakage current measured as shown in Fig. 3 with a constant V_{ds} of 1 V and shows that the inverse subthresh-

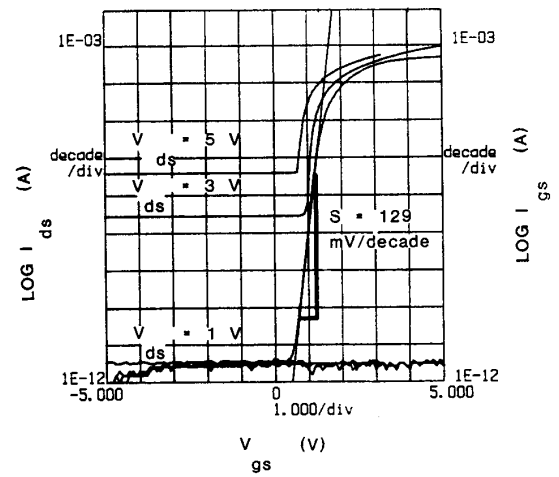

Fig. 3. Plots of log I_{ds} versus V_{gs} with V_{ds} = 1, 3, and 5 V for the device of Fig. 2.

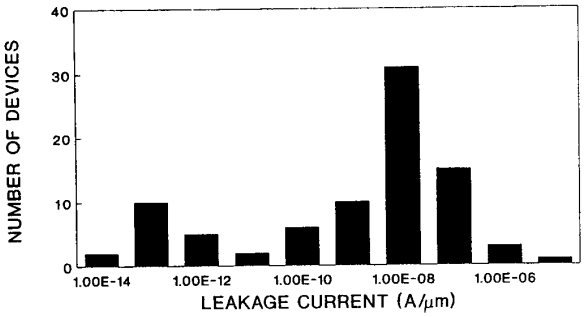

Fig. 4. The number of devices at each order of magnitude of leakage current across a typical electron-beam ZMR wafer.

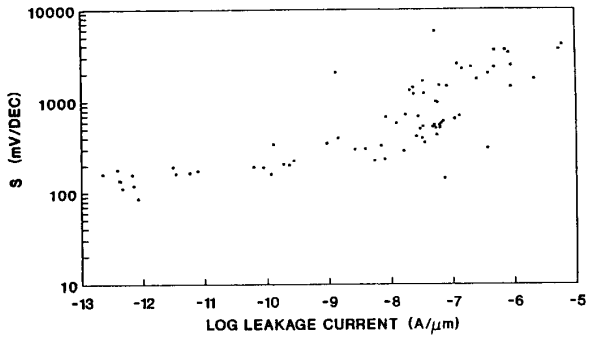

Fig. 5. Plot of log inverse subthreshold slope versus log leakage current normalized to W for a constant V_{ds} of 1 V.

old slope remains less than 200 mV/decade when leakage currents are below 10^{-9} A/μm. The inverse subthreshold slope increases dramatically to greater than 200 mV/decade when leakage current rises above 10^{-9} A/μm. Similarly, Fig. 6, a semi-log plot of V_t versus leakage current normalized to W and found using the intercept technique shows that the value of V_t is independent of leakage current with a mean and standard deviation of

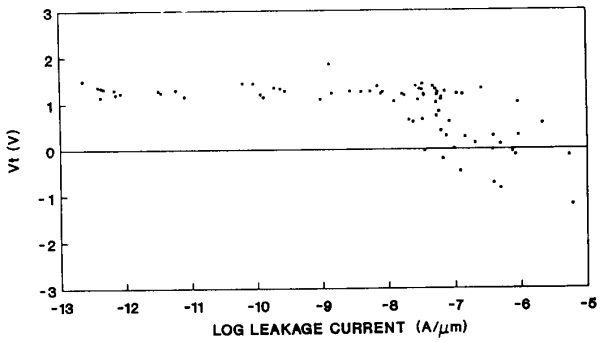

Fig. 6. A plot of measured V_t versus log leakage current, normalized to W.

1.2 $\pm$ 0.5 V when leakage currents are below approximately 10^{-8} A/μm. The experimental value of V_t decreases monotonically to negative values when the leakage current increases above 10^{-8} A/μm.

The excessively large off-state leakage current cannot be accounted for by leakage through the gate oxide, since the gate current (I_{gs}) remains well below that of I_{ds} throughout the I_{ds}–V_{gs} scan; for example, a device with an I_{ds} leakage current of 8×10^{-8} A/μm has an I_{gs} leakage current of < 1 ρA (at our noise limit). The leakage is also not due to a "short-channel" effect since the leakage current is independent of channel length for the devices studied here. Thus to better determine the origin of the off-state leakage current, temperature and voltage dependencies of the current flow (I_{ds}) through the drain-to-body and source-to-body n^+-p junctions of devices exhibiting various leakage currents have been investigated.

Fig. 7 compares junction current flow under reverse-bias conditions (i.e., $V_{ds} \leq 5$ V, $V_{gs} = 0$ V) for devices with high (10^{-8}-A/μm) and low (10^{-13}-A/μm) leakage currents. The drain-to-body (source grounded) reverse-bias current (I_r) for the device with high I_L has a significantly stronger reverse-bias dependence and a lesser forward-bias dependence than does the device with low I_L. No significant differences could be determined in the values of I_r measured either between drain-to-body or source-to-body by switching the ground contact.

The temperature dependence of I_r is measured for the devices of Fig. 7 by monitoring the value of I_{ds} as the temperature of the device is increased from 25°C to 250°C with $V_{ds} = 1$ V and $V_{gs} = 0$ V as shown in the semi-log plots of current density versus $1/T$ in Fig. 8. Activation energies (E_a) have been calculated from the slope of the linear region of the Arrhenius plots of Fig. 8 for both a high-leakage and a low-leakage device. The high-leakage device whose characteristics are plotted in Fig. 8 has an I_r which is relatively insensitive to changes in temperature with an E_a of 0.2 eV. The leaky devices do not, however, appear to have a singular E_a value as another device with a leakage current of approximately 1×10^{-8} A/μm exhibited an E_a of 0.63 eV. For devices with low leakage, I_r varies significantly with temperature and has a discrete

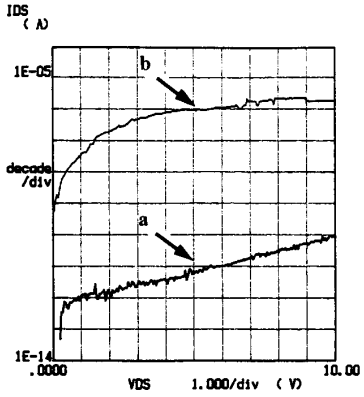

Fig. 7. Junction current flow under both forward- and reverse-bias conditions (i.e., V_{ds} from -1 to 1 V, V_{gs} = 0 V) for devices with *a* low and *b* high leakage currents.

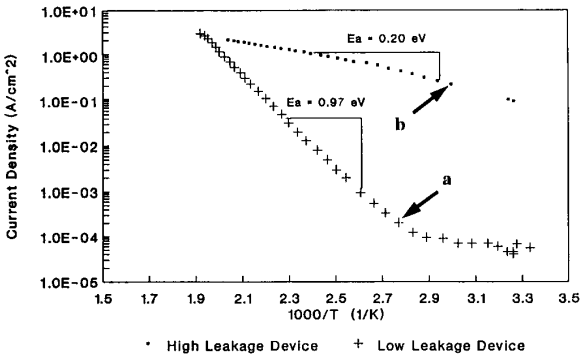

Fig. 8. Temperature dependence from 25°C to 250°C of the current flow under reverse-bias conditions (i.e., V_{ds} = 1 V and V_{gs} = 0 V) for devices of Fig. 7 with *a* low leakage current and *b* high leakage current.

E_a of approximately 0.97 eV (close to that expected for band-to-band transitions in Si).

The effective electron surface mobility as determined from values of an I_{ds} versus V_{gs} curve with V_{ds} = 0.1 V via 3) for the device of Fig. 2 exhibits a peak mobility value of 898 $cm^2/V \cdot s$. The peak mobility value for a higher leakage current device is 697 $cm^2/V \cdot s$. This discrepancy cannot be accounted for solely by utilizing an effective gate length (L_{eff}) in (3), where L_{eff} is the mask gate length L reduced by a ΔL due to encroachment into the channel region during pattern definition of the source and drain regions. Following the Terada and Muta method [19] as suggested by Ng and Brews [20], we estimated a reduction in channel length (ΔL) from the mask channel length (L) for the devices discussed to be 0.225 μm by comparing the value of I_{ds}/V_{ds} at different values of V_{gs} in the linear region. By substituting the effective channel length ($L_{eff} = L - \Delta L$) into (3) for the mask channel length, the mobility is theoretically decreased only slightly for the low leakage device of Fig. 2 (L = 3 μm, $L_{eff} \simeq$ 2.7 μm) to 825 $cm^2/V \cdot s$ which is still higher than 697 $cm^2/V \cdot s$ calculated for the high-leakage device (L = 40 μm, $L_{eff} \simeq$ 39.7 μm).

V. Interpretation of Results

Table I summarizes the characteristics of two typical electron-beam ZMR SOI NMOS devices exhibiting different leakage currents. Appropriate values for a bulk silicon NMOS transistor are also listed in Table I. It is apparent that high leakage current significantly degrades the transistor turn-on characteristics. Since the source of the leakage current is not the gate oxide, the drain-to-body and source-to-body n^+-p junctions are suspect. Possible mechanisms which could explain the high leakage current are discussed next.

The drain-to-body (source grounded) I_r for a leaky device has a strong dependence on V_{ds} suggesting that generation of carriers within the space-charge region dominates over diffusion current from the body. Leakage current is independent of channel length which rules out a space-charge-limited current-flow mechanism. The reverse-bias leakage current for a highly leaky device is not strongly dependent upon temperature with a activation energy of 0.2 eV. Thus the leakage current is probably not associated with the thermal emission of carriers from metallic impurities whose energy states are discrete and lie deeper in the bandgap than 0.2 eV (e.g., Cr = 0.41 eV, Fe = 0.51 eV) [18]. Both field emission [21] and thermionic field emission [22] of trapped charge from grain boundaries has explained leakage currents exhibited in polysilicon MOSFET's. Thermionic field emission could be the dominant mechanism creating the excessive leakage current values exhibited by many of the ZMR SOI MOSFET's examined here as it is consistent with the significant dependence on reverse bias of I_r for the leaky devices and with the varied dependence upon temperature.

It has been shown previously that the crystallographic quality of the electron-beam ZMR SOI material is disrupted by subgrain boundaries. These boundaries are oriented at a 45° angle with respect to the MOSFET's and have a characteristic spacing ranging from 20 to 100 μm. The spacing depends upon the recrystallization conditions but the precise subgrain boundary location is uncontrolled in these SOI wafers. Thus because our MOSFET's have dimensions on the order of the boundary spacing, it is expected that many devices intersect one or more boundaries somewhere within the channel region. The subgrain boundaries can be observed optically via Nomarski differential contrast microscopy in regions of the wafer where the field oxide is exposed. A correlation between the number of subgrain boundaries crossing a MOSFET and the magnitude of the devices' leakage current has been attempted but was inconclusive. Even if each subgrain boundary could be accounted for, optical microscopy cannot quantify the planar deviation and density of defects within the boundaries which must ultimately determine the effect on the leakage current. Also impurities such as carbon, which are known to be present, may segregate into the defective subgrain boundaries which could also affect the leakage current. We therefore conclude that the leakage current is due to the defects and impurities lying

TABLE I
SUMMARY OF THE CHARACTERISTICS OF TWO TYPICAL ELECTRON-BEAM ZMR SOI DEVICES (ONE WITH HIGH AND ONE WITH LOW OFF-STATE LEAKAGE CURRENT) TOGETHER WITH APPROPRIATE VALUES FOR A BULK SILICON NMOS TRANSISTOR

Device	I_L (A/μm)	V_t (V)	Q_s (#/cm^2)	S (mV/dec)	E_a (eV)	μ_n (cm^2/V · s)
SOI	8×10^{-8}	0.6	$+1.4 \times 10^{11}$	1620	0.2	693
SOI	$<1 \times 10^{-12}$	1.2	-1.8×10^{10}	131	0.9	823
BULK	$<1 \times 10^{-12}$	0.8	$< \pm 1 \times 10^{10}$	120	1.1	1200

within these subgrain boundaries and we expect a higher yield of idealistic devices if both the crystallographic quality can be improved in uniformity across the wafer and the impurity concentration can be reduced.

VI. CONCLUSIONS

NMOSFET's have been fabricated in electron-beam-recrystallized SOI layers and their electrical characteristics have been examined. Despite the immaturity of the electron-beam recrystallization method, the effective mobility and subthreshold slope for some devices approach those of bulk Si. More work is required to reduce impurities especially carbon. Defect levels appear to be degrading the devices' leakage currents causing undesired shifts in V_t and increasing the inverse subthreshold slope.

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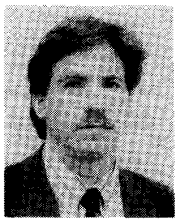

Lance R. Thompson (S'83-M'83-M'85-S'87-M'89-S'90-M'90-S'91-M'91) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Colorado State University, Ft. Collins, in 1983, 1986, and 1991, respectively.

As a graduate student he spent some time at NASA Lewis Research Center studying laser-assisted CVD of insulators on III-V compounds. He also performed the majority of his Ph.D. dissertation at Sandia National Laboratories investigating electron-beam recrystallization of SOI layers. He is now a Development Engineer at Storage Technology Corporation, Louisville, CO. He has published over 20 journal and conference papers in microelectronic materials processing and characterization. His current research interests center on optoelectronic data communications.

James R. Buser (S'87-M'92) was born in Pittsburgh, PA, in 1955. He received the B.A. degree in music from Indiana University of Pennsylvania, Indiana, PA, in 1977 and the B.S. degree in electrical engineering from Colorado State University, Fort Collins, in 1991.

Among his current interests are semiconductor manufacturing processes, materials science, and optoelectronics. He works with students at Front Range Community College on a variety of electronics topics and is employed at Hewlett-Packard in a surface mount facility.

Mr. Buser is a member of the IEEE Lasers and Electro-Optics Society and the IEEE Aerospace and Electronic Systems Society. He was secretary and, later, vice president of the student chapter of IEEE while attending Colorado State. One of his achievements was winning the local IEEE student paper contest.

Jack D. Meyer (S'83-M'83-S'84-M'86) received the B.S., M.S., and Ph.D. degrees in electrical engineering, all from Colorado State University, Fort Collins.

He developed electron-beam processes while employed by Applied Electron Corporation, Albuquerque, NM, and now investigates plasma processing at Quantum Research Corporation, Fort Collins, CO.

Cameron A. Moore (S'82-M'84-S'85-M'85-M'86) received the B.S. degree in physics from the University of Southern California, Los Angeles, and the M.S. and Ph.D. degrees in electrical engineering from Colorado State University, Fort Collins.

During his graduate studies he was a visiting student at Sandia National Laboratories, Albuquerque, NM and at Bell Laboratories, Murray Hill, NJ. He has held positions at Plasma and Materials Technologies, Applied Electron Corporation, NCR Microelectronics, and Hughes Aircraft Co. He is currently an Assistant Professor in the Department of Engineering at the University of Denver, Denver, CO. His current research interests include SOI materials and devices, thin-film processing, vacuum microelectronics, nanostructures, and silicon optoelectronics.

Jay T. Fukumoto (M'84-M'90) received the B.S. degree in electrical engineering from the University of Illinois, Urbana-Champaign.

He was previously employed by Applied Electron Corporation developing SOI technology. He is currently employed as a Process Engineer at NCR Microelectronics Corporation, Fort Collins, CO.

George J. Collins (S'62-M'72-SM'75-F'87) graduated from Yale University, New Haven, CT.

He is a Professor of Electrical Engineering at Colorado State University, Fort Collins. He has served as a Consultant to both industry and government, including Bell Laboratories, NCR, Lawrence Livermore National Laboratory, the National Bureau of Standards, Lasertechnics (Albuquerque, NM), and the Applied Electron Corporation (Santa Clara, CA). Prior to joining Colorado State University, he was a Research Associate at the Dunham Laboratory, Oxford University, and a Visiting Scientist under the U.S.-Japan Cooperative Science Program at Nagoya University. He is the author of more than 100 technical papers.

Dr. Collins is a member of the American Physical Society, Eta Kappa Nu, Sigma Xi, Sloan Foundation Fellow (Physics), and is a recipient of the Halliburton Award.