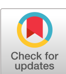

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RESEARCH-ARTICLE

Page-Overwrite Data Sanitization in 3D NAND Flash: Challenges, Feasibility, and the PULSE Solution

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Page-Overwrite Data Sanitization in 3D NAND Flash: Challenges, Feasibility, and the PULSE Solution

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Instant data deletion (or sanitization) in NAND flash devices is essential for achieving data privacy, but it remains challenging due to the mismatch between erase and write granularities, which leads to high overhead and accelerated wear. While page-overwrite-based instant data sanitization has proven effective for 2D NAND, its applicability to 3D NAND is limited due to the unique sub-block architecture. In this study, we experimentally evaluate page-overwrite-based sanitization on commercial 3D NAND flash memory chips and uncover significant threshold voltage disturbances in erased cells on adjacent pages within the same layer but across different sub-blocks. Our key findings reveal that page-overwrite sanitization increases the median raw bit error rate (RBER) beyond correction limits (exceeding 0.93%) in Floating-Gate (FG) Single-Level Cell (SLC) technology, whereas Charge-Trap (CT) SLC 3D NAND flash memories exhibit higher robustness. In Triple-Level Cell (TLC) 3D NAND, page-overwrite sanitization proves impractical, with the median RBER of ~13% for FG and ~5% for CT devices. To overcome these challenges, we propose **PULSE**, a low-disturbance sanitization technique that balances sanitization efficiency (η_{san}) and data integrity (RBER). Experimental results show that PULSE eliminates RBER increases in SLC devices and reduces the median RBER to below 0.57% for FG and 0.79% for CT in fresh TLC blocks, demonstrating its practical viability for 3D NAND flash sanitization.

CCS Concepts: • **Hardware;** • **Security and privacy** → **Security in hardware;** • **Information systems** → **Information storage systems**;

Additional Key Words and Phrases: Flash memories, 3D NAND, data sanitization

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1 Introduction

With flash memory widely used in smartphones, SD cards, USB drives, and SSDs, secure and immediate data sanitization has become critical to protect user privacy. The **Data Protection Act** (**DPA**) 2018 [35] mandates absolute deletion from storage devices, data should be irrecoverable by any means. However, standard sanitization methods often fail short [9, 27, 28, 18, 32], leaving sensitive information vulnerable to recovery. A recent report by Blancco Technology Group found that 42% of used SSDs sold on eBay contained recoverable data despite being "sanitized" [11, 36], highlighting a key issue: users may attempt to sanitize their devices, but the methods they rely on are often ineffective, particularly in flash-based storage systems.

Instant sanitization in NAND flash memory involves erasing sensitive data at the page level, the smallest addressable storage unit. However, this is complicated by the architecture and operational constraints in flash memory. NAND flash is organized into blocks, and each block contains hundreds of pages. While pages are the unit of read and write operations, erasure occurs only at the block level. Additionally, NAND flash follows an erase-before-write protocol, meaning a page cannot be overwritten unless the entire block is first erased. Since erasing a block requires migrating all valid pages to a new location, in-place updates are impractical. Instead, new data is written to a free page, and the old page is simply "unlinked" or marked invalid. However, the invalidated data physically remains in the medium, posing a privacy risk.

To manage the granularity mismatch between logical and physical operations, flash-based storage systems rely on an intermediate firmware layer called the **Flash Translation Layer** (**FTL**). The FTL, running on the flash memory controller, handles address mapping, wear leveling, garbage collection, and error correction. Typically, invalid data is removed during garbage collection via block erasure, but this process is deferred to minimize overhead. A major drawback of using the block erasure and garbage collection routine for instant sanitization is its poor performance caused by significant overhead due to valid data migration [6, 30, 31] and long latency associated with block erase commands. In addition, this technique increases wear and thus limits the effective capacity/operating time of storage systems. Consequently, the FTL postpones the use of garbage collection routines, allowing for invalid data to persist on flash media long after the initial deletion, delaying effective data sanitization.

To address these challenges and enable page-level instant sanitization in flash-based storage, a page-overwrite method using all-zeros was introduced by Wei et al. [33] and subsequently refined by others [3, 10, 14, 26]. This method has proven effective for 2D NAND. However, adapting it to 3D NAND introduces new complications. In 3D NAND, pages in the same vertical layer share the same **word line** (**WL**) but belong to different physical **sub-blocks** (**SBs**). Consequently, overwriting one page can inadvertently impact data integrity in other pages sharing the same WL across SBs. Furthermore, instant sanitization based on page-overwrite has mostly been explored for **single-level cell** (**SLC**) NAND [33] and **multi-level cell** (**MLC**) [26], while many modern storage devices use higher-density **triple-level cell** (**TLC**) technology. Thus, the efficacy of overwrite-based sanitization in 3D NAND with logically scaled storage media remains an open question.

This article presents the first experimental evaluation of overwrite-based page-level sanitization for 3D NAND with SLC and TLC configurations, using **commercial-off-the-shelf** (**COTS**) 3D NAND chips from three different vendors. Our key findings include:

— Overwrite sanitization achieves $\eta_{san} \approx 100\%$ in both **charge-trap** (**CT**) and **floating-gate** (**FG**) 64-layer SLC 3D NAND chips, leaving no traces of original data on the target pages.
— For the first time, we demonstrate overwrite sanitization on TLC 3D NAND chips, where three shared pages are sanitized together, achieving $\eta_{san} \approx 100\%$ in both CT/FG NAND chips.
— Overwrite sanitization increases RBER on adjacent valid pages sharing the same WL as the sanitized page. In 64-layer FG SLC 3D NAND, the median RBER can exceed 0.93%, surpassing standard **Error Correction Code** (**ECC**) correction limits. In contrast, 64-layer CT SLC NAND shows strong resilience, with zero RBER observed even under worst-case scenarios.
— Our analysis of post-sanitization disturbances reveals that a significant up-shift of the erase threshold voltage (V_{th}) distribution of valid data pages is the root-cause for data corruption. The disturbance effects are more severe in the middle layers of the 3D stack. Although CT SLC chips demonstrate greater resilience, V_{th} distribution measurements confirm that the underlying disturbance mechanism is consistent across both FG and CT technologies.
— In TLC 3D NAND, overwrite sanitization results in severe RBER increases on the valid flash memory pages for both CT and FG technology (RBER (median) ~5% (CT) and ~13% (FG)), making it impractical on TLC devices.

To address these limitations, we propose **PULSE**, a Partial Update-based Low-disturbance Sanitization Engine that balances sanitization efficiency and data integrity in 3D NAND. PULSE leverages partial programming to minimize disturbance to neighboring cells holding valid data, while still removing the invalid data from the target pages. Experimental evaluation shows that:

— In SLC flash (both FG and CT types), the increase in RBER for valid data remains negligible and well below the ECC correction threshold, while invalid data is effectively sanitized using the PULSE method.
— In TLC flash, PULSE reduces the median RBER to less than 0.79% for CT and 0.57% for FG 64-layer 3D NAND chips while ensuring $\eta_{san} > 90\%$ on the invalid pages.

The rest of the paper is organized as follows. Section 2 provides background information on 3D NAND architecture. Section 3 reviews related work. Section 4 discusses the challenges associated with overwrite sanitization in 3D NAND. Section 5 describes experimental evaluation and characterization results. Section 6 introduces PULSE sanitization and its experimental evaluation on both SLC and TLC flash memories, while Section 7 discusses the implications of PULSE in the future 3D NAND design. Finally, Section 8 concludes the paper.

2 Background

This subsection provides a brief overview of the 3D NAND flash SB architecture and compares FG and CT NAND flash technologies to enhance the understanding of NAND flash memory.

2.1 Sub-block Architecture of 3D NAND

3D NAND flash memory achieves a high bit density by vertically stacking multiple layers of flash memory cells. Figure 1(a) illustrates the physical organization of a 3D NAND flash memory block. The green layers represent the WLs in the flash memory array, while the red bars at the top denote the **bit lines** (**BLs**). The purple pillars are the polysilicon channels, and the blue region at the bottom represents the silicon substrate. The yellow bars on top of the substrate correspond to the **source select gate** (**SSG**) transistors, and a similar yellow bar near the BLs represents the **drain select gate (DSG)** transistors.

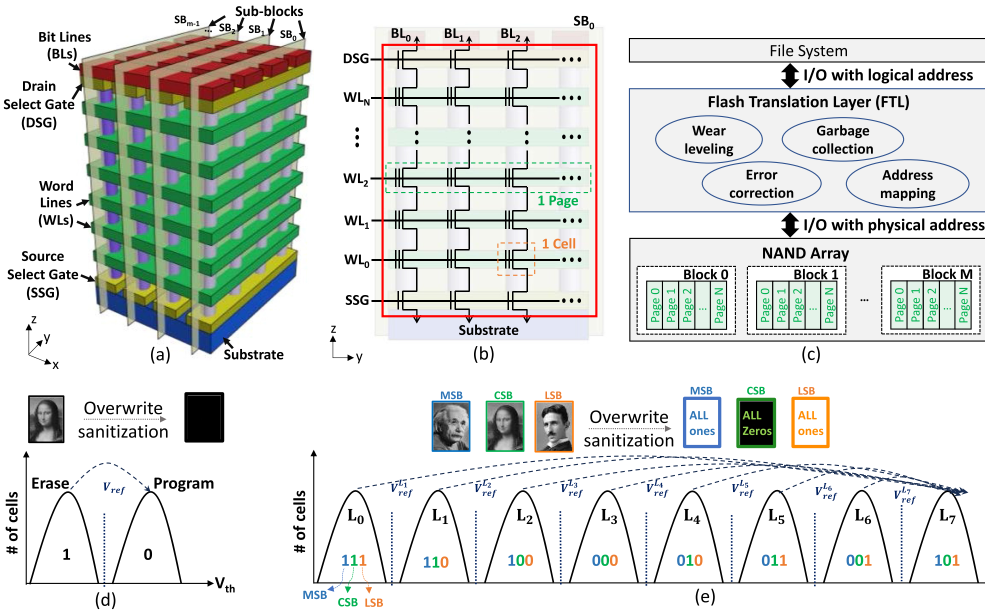

Fig. 1. (a) Physical structure of a 3D NAND flash memory array. (b) Circuit schematic of a 3D NAND flash SB. (c) System view of NAND flash storage. The cell V_{th} distribution in (d) SLC, and (e) TLC storage with corresponding overwrite sanitization scheme.

A 3D NAND block is physically divided into several SBs to optimize the die area utilization [1]. Each SB comprises all the purple poly-silicon pillars along the same y-axis, as shown in Figure 1(a). Within a SB, the pillars connect to the substrate when the SSG bar is activated and to individual BLs when the corresponding DSGs are turned on. SBs are structurally identical, and SSG transistors enable the selection of a specific SB during page read and write operations. However, all SBs are simultaneously erased during a block erase operation. Figure 1(b) shows the circuit schematic of a SB. Each SB consists of multiple flash pages, typically 16 KB per page in state-of-the-art 3D NAND chips. All cells in the same row share a common WL. The cells in a vertical column connect to a metal BL through their DSG and to ground via their SSG. Note that each flash memory layer corresponds to a metal WL; hence, the terms are used interchangeably in this article.

Commercially available 3D NAND chips primarily employ two types of storage elements: FG and CT cells. In FG cells, a poly-Si conductive storage node serves as an isolated island surrounded by dielectric layers. In contrast, CT cells utilize a continuous silicon nitride (Si_3N_4) storage layer that traps electric charges in densely distributed trap sites. CT cell technology, enabled by its distinctive gate-last processing steps, offers inherent advantages for future scalability. As a result, industry trends are shifting towards adopting CT cell structures for the next generation of 3D NAND flash memory.

2.2 Reliability Management by Flash Translation Layer (FTL)

Flash-based storage systems consist of a controller and one or more flash memory chips. The flash controller manages the flash media on one side and interfaces with the host on the other, as shown in Figure 1(c). It executes an intermediate firmware layer known as FTL [2, 34]. The FTL comprises multiple modules responsible for: (1) mapping logical block addresses to physical addresses in the flash media; (2) performing wear leveling to ensure that all blocks degrade

uniformly; (3) conducting garbage collection by tracking invalid pages and selecting blocks for erasure when the number of free blocks falls below a threshold; and (4) applying error correction, enabling a certain number of errors in the flash media to be corrected [2].

2.3 Threshold Voltage (V_{th}) Distribution of SLC and TLC Storage

SLC flash memory stores one bit per cell and can exist in two distinct V_{th} states, as shown in Figure 1(d). The read reference voltage (V_{ref}) is set between the erased and programmed state distributions, ensuring sufficient noise margin for reliable state identification. SLC flash memory is highly reliable due to the large V_{th} margin between states [8]. Overwrite sanitization of an SLC flash page is achieved by programming all cells into the programmed state, as illustrated using the Mona Lisa image in Figure 1(d).

Modern flash memory technologies store multiple bits per cell, including MLC (2 bits), TLC (3 bits), **Quad-Level Cell** (**QLC**, 4 bits), and **Penta-Level Cell** (**PLC**, 5 bits) [7, 12]. In TLC flash memory, each cell stores three bits, which means that each physical WL contains three logical pages. The **most significant bits** (**MSB**) of all cells on a given WL form the logical MSB page, while the **least significant bits** (**LSB**) and **central significant bits** (**CSB**) form the LSB and CSB pages, respectively [20, 25].

Because each TLC cell stores three bits, it must support eight distinct V_{th} levels (L_0–L_7) during programming. The digital interpretation of a cell's V_{th} state depends on the encoding scheme, typically Gray coding, which minimizes bit errors by ensuring that adjacent voltage states differ by only one bit [5, 21]. Figure 1(e) illustrates a Gray-coded TLC scheme. A cell's final V_{th} value is determined by the combination of values stored in the three logical pages. For example, if the MSB page contains all ones, the CSB page contains all zeros, and the LSB page contains all ones, the corresponding flash memory cells are programmed to the L_7 state. Overwrite sanitization in TLC flash memory can be implemented by programming all cells to the highest V_{th} state (L_7), which simultaneously sanitizes all three shared logical pages (LSB, CSB, and MSB), as shown in Figure 1(e).

3 Related Work

Several data sanitization methods have been proposed for NAND flash storage systems in recent years to enhance data privacy. We summarize these approaches below.

3.1 Block Erase

Block erasure is a basic NAND command used to remove data from all pages in a flash block (Figure 2(c)). This method physically erases data by discharging all cells in the block. Typically, the garbage collection function of the FTL uses this method to remove old, invalid data when the drive is nearly full. A major drawback of block erasure for *instant sanitization* is its poor performance, which is caused by significant overhead due to valid data migration [6, 30, 31], and a block erase operation that takes more time than a page program operation. In addition, frequent block erasures contribute to accelerated wear-out, reducing the effective capacity and lifespan of the flash device. As a result, modern flash controllers invoke this command sparingly.

3.2 Logical Data Deletion

To avoid performance penalties of block erasure, NAND flash controllers typically perform logical data deletion by invalidating the page addresses of obsolete data [22, 24, 34]. This process is managed by the FTL, which maps logical pages to physical ones. Thus, for any page update operation, the FTL will write the new content to a fresh physical page (or block) and update the address map table to point to the new page. The old data, however, remains physically present in the storage

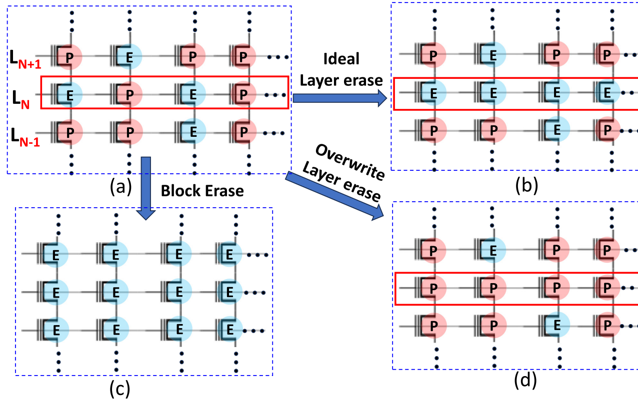

Fig. 2. (a) A schematic of an SLC NAND block containing random data, where each row is a page. (b) Ideal page erase, (c) block erase, and (d) overwrite page erase. Cells in 'E' state represent logic 1 while cells in 'P' state represent logic 0.

medium. Since this invalidated data can still be retrieved using advanced memory access tools, logical deletion does not provide true data sanitization and poses a security risk.

3.3 Overwrite-based Page Sanitization

To achieve page-level instant data sanitization, Wei et al. [33] proposed a "data scrubbing" approach, which was later refined by others [3, 4, 10, 14, 19, 32]. This method reprograms a page with all-zero data (Figure 2(d)), effectively sanitizing the contents by overwriting them. While effective for 2D NAND and SLC-based devices, overwrite-based sanitization has not been thoroughly evaluated in the context of 3D NAND, which introduces architectural complexities such as SB structures. In this article, we present the first experimental validation of this technique across multiple types of 3D NAND flash devices (FG, CT) and different cell densities (SLC, TLC).

3.4 Encryption-based Data Deletion

Encryption-based deletion techniques have also been proposed to achieve secure data removal [18, 27–29]. These methods encrypt the user file with an encryption key and store the encrypted data and the key in two separate NAND blocks. Secure data deletion is achieved by erasing the keys, which can be done efficiently as keys require less space in memory. Even though encryption-based techniques are promising, they suffer from several drawbacks. First, the encryption-based deletion method carries the risk of data recovery, as its implementation may have certain issues, e.g., random number generation (for the encryption key) that can be compromised by a motivated adversary. Second, encryption-based deletion requires the proper removal of encryption keys and any other derived values that might be useful in cryptanalysis. Third, many existing storage systems and embedded platforms do not include hardware modules for accelerating encryption/decryption tasks and rely on software solutions that can severely degrade system performance.

3.5 Evanesco

Kim et al. [16] introduced Evanesco, a hardware-supported technique for efficient data sanitization in modern flash-based storage systems. Evanesco sanitizes data by blocking access to invalidated data, either at the page or block level. While this approach is highly effective, the data stored in the flash medium is not physically removed, making it susceptible to future direct or indirect data retrieval attacks.

Table 1. Comparison of Different Sanitization Methods

Methods	Security guarantee	Data reliability	Performance overhead	Implementation complexity
Block erase	High	High	High	Low
Logical deletion	Low	High	Low	Low
Full overwrite	High	Low	Moderate	Low
Encryption	Moderate	High	Low	High
Evanesco	Moderate	High	Low	High
PULSE	High	High	Moderate	Low

In summary, different sanitization techniques have been proposed in prior work, each offering different trade-offs among security, data reliability, performance overhead, and hardware implementation complexity. Table 1 summarizes and compares the key sanitization methods. As demonstrated in this work, traditional overwrite sanitization enables fast and secure data deletion with minimal performance cost, but it introduces disturbances to nearby valid pages in a 3D NAND array, compromising data integrity. In contrast, PULSE provides strong security guarantees and robust data reliability, while incurring only moderate performance overhead. These advantages make PULSE a compelling solution for secure and low-disturbance data sanitization in contemporary 3D NAND flash memory systems.

4 Technical Challenges and Contributions

4.1 Technical Challenges Associated with Overwrite Sanitization in 3D NAND

Figure 3 illustrates a simplified 3D NAND memory block and the biasing scheme during a page overwrite operation. The block consists of m physical SBs, each consisting of multiple pages, some holding valid data (green) and others marked as invalid (red). For example, in Figure 3, page-2 of SB-0 is invalid and is being sanitized using an all-zero overwrite operation. During the page program operation, a high programming voltage (V_{pgm} > 20V) is applied to the selected WL, while unselected WLs are held at a moderate pass voltage (V_{pass} ≈ 8V). This biasing can cause weak program disturbance effects, particularly in erased cells within the block. The highest risk is valid pages that share the same WL as the overwritten page (outlined with a red border in Figure 3), which are directly exposed to V_{pgm}. Additionally, pages in adjacent layers (outlined with a yellow border) may also experience moderate interference effects due to capacitive coupling.

It is important to note that 2D NAND technology does not incorporate the sub-block flash memory architecture, limiting disturbances during overwrite sanitization to manageable interference effects (Figure 3, yellow) without any direct disturbances (Figure 3, red). Previous studies [6, 30, 31], [33] have shown that these interference effects in 2D NAND, particularly in SLC configurations, can be mitigated using standard ECC mechanisms, enabling the successful implementation of overwrite sanitization. However, this approach does not directly translate to 3D NAND technology, which invariably features sub-block architectures. Overwrite operations in 3D NAND result in not only interference effects but also direct programming effects on valid flash memory pages sharing the same WL. These direct disturbances significantly complicate the implementation of overwrite sanitization, requiring careful evaluation to maintain data integrity.

4.2 Contributions of this Article

This article addresses the above challenges and introduces novel contributions that advance the field of instant sanitization of NAND flash memory:

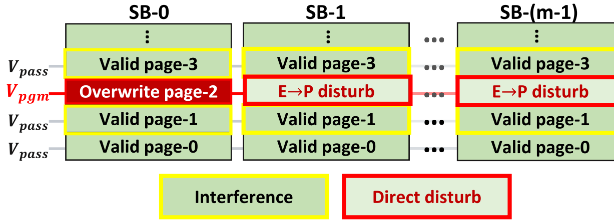

Fig. 3. Biasing scheme during page-overwrite operation and corresponding disturbances on valid flash pages in 3D NAND SBs.

- **First experimental evaluation of overwrite sanitization in 3D NAND**: While prior studies on overwrite sanitization have primarily focused on 2D SLC NAND, our work is the first to experimentally investigate this process in modern 3D NAND devices. Through detailed threshold-voltage measurements and error characterization, we uncover previously unexplored post-sanitization disturbance effects on valid data. These effects are strongly influenced by the unique SB organization of 3D NAND and by layer-specific interactions within the vertical stack, leading to non-uniform susceptibility across layers. Our findings highlight critical reliability concerns that are absent or less pronounced in planar NAND, providing new insights for the design of secure and disturbance-resilient sanitization methods in 3D flash technologies.
- **First experimental evaluation of overwrite sanitization in TLC NAND**: Overwrite sanitization has been studied mainly in SLC and MLC NAND flash. This work is the first to demonstrate overwrite sanitization in TLC NAND, exposing the complications that arise when sanitizing all three logical pages (LSB, CSB, and MSB) simultaneously.
- **Proposal of the PULSE sanitization technique**: We introduce PULSE, a novel sanitization method designed to reduce post-sanitization disturbance on valid data, while achieving effective sanitization of invalid data. Through experimental validation on multiple 3D NAND chips, we establish practical guidelines for integrating PULSE into future 3D NAND architectures. Our findings lay a strong foundation for implementing overwrite sanitization in next-generation 3D NAND SSDs, ensuring instant data deletion and mitigating data leakage—an essential security concern for SSDs.

5 Experimental Evaluation

5.1 Experimental Set-up and Implementation

Our experimental evaluation is conducted on multiple 3D NAND memory chips sourced from three major NAND manufacturers. A custom-designed test board used in our evaluation is shown in Figure 4(a). It consists of a 132 **Ball-Grid-Array** (**BGA**) socket to hold a flash memory chip and an FT2232H mini module that connects the 3D NAND chip to a workstation via a **Universal Serial Bus** (**USB**) interface. A software package running on the workstation executes **Open NAND Flash Interface** (**ONFI**) commands to perform the low-level flash memory operations, such as page read, page write, and block erase.

Overwrite sanitization in this study is implemented using the user-mode page write command with an all-zero data pattern. The raw NAND chips support out-of-order page write operations and do not include any internal data scramblers, data randomizer engines, or on-chip ECC engines. These functionalities are typically handled at the storage controller level, depending on application needs. For chips equipped with an on-chip ECC engine or data randomizer, standard user-mode

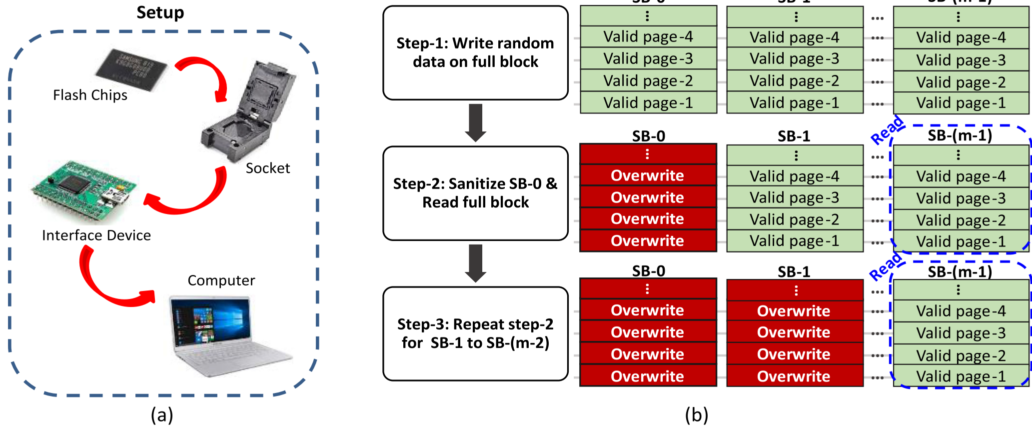

Fig. 4. (a) Experimental setup. (b) Experimental flow for evaluating sanitization efficiency and disturbance effects.

commands may not suffice for implementing overwrite sanitization, and assistance from the chip manufacturer may be required.

Figure 4(b) illustrates the experimental flow used to evaluate the effects of overwrite sanitization on both valid and invalid pages within a 3D NAND block. The process begins by writing random data to all flash pages in the block, followed by a verification step using page reads to confirm a zero ***raw bit error rate*** (**RBER**). Next, overwrite sanitization is performed page-by-page. For systematic evaluation, we first sanitize all flash pages within SB-0, then read all pages of the block. The sanitization effectiveness is quantified by comparing the sanitized page content to a predefined solid data pattern, typically an all-zero or all-one pattern, depending on the logical page type and the NAND operating mode. *Sanitization efficiency of invalid pages* (η_{san}^{inval}) is defined as:

$$\eta_{san}^{inval} = \frac{Invalid_{data}\ \ XNOR\ Solid_{data-pattern}}{Page_{size}} \times 100\%. \tag{1}$$

Here, the solid data pattern represents the expected post-sanitization content (e.g., all-zeros or all-ones). For example, in an SLC page, the solid data pattern is all-zeros. In contrast, for TLC storage where the highest V_{th} state is encoded as "101," the solid data pattern corresponds to all-ones for the MSB and LSB pages, while the CSB page retains an all-zero pattern. Note that a 100% sanitization efficiency indicates that the invalid page data has been fully converted into a solid data pattern, and hence, the data is logically irrecoverable.

Simultaneously, disturbances on valid pages are measured by calculating the RBER relative to their original data patterns. This process is repeated for each SB, except for the last one. The last SB typically experiences the worst-case disturbance due to cumulative interference from previous operations. To quantify this, we evaluate the RBER of valid pages in the last SB, which offers insight into the most severe reliability challenges posed by overwrite sanitization. In the following subsections, we present detailed experimental observations for three types of 3D NAND flash memory: SLC (Section 5.2-5.3), and TLC CT and FG-based (Section 5.4).

5.2 Evaluation of Sanitization in SLC FG 3D NAND

5.2.1 Evaluation of Sanitization Efficiency on Invalid Target Pages. Figure 5(a) visually demonstrates the effectiveness of the overwrite sanitization technique on an invalid page (or a target

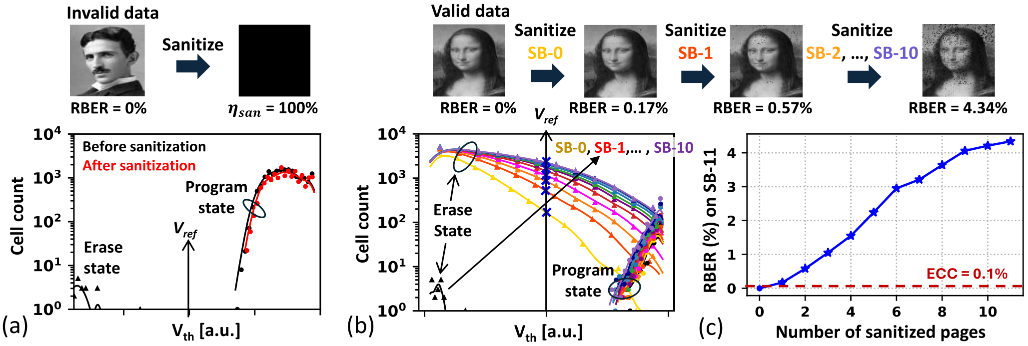

Fig. 5. (a) Evaluation of overwrite sanitization on an invalid page. Before sanitization, the page contains a tesla image, and after sanitization, it is converted to a perfect black image (η_{san} = 100%). The corresponding V_{th} distribution before (black) and after (red) sanitization. (b) Evaluation of the sanitization impact on the valid page of the same layer and the corresponding V_{th} distributions. (c) The RBER values on the valid page plotted against the number of sanitized pages within the same layer.

page) storing a Tesla image. After applying the sanitization operation, the image is transformed into a fully black, all-zero pattern, confirming the successful sanitization of the invalid flash memory page. To validate this not only at the data level but also at the physical level, we measure the V_{th} distribution using the Read-offset command [37].

The plot in Figure 5(a) shows the measured V_{th} distribution from an SLC page, capturing both the erase and program states. The V_{th} values are expressed in **arbitrary units (a.u.)**, as the absolute value of the reference voltage is not disclosed in the chip's datasheet. Due to the limited range of the Read-offset command, only the upper tail of the erase state and the lower tail of the program state are captured. The black curve represents the V_{th} distribution of the original data before sanitization, while the red curve shows the sanitized state. The vertical arrow marks V_{ref}, applied to the WL to sense cell states during read operations. The significant margin between V_{ref} and the erase/program distribution tails ensures a zero RBER. Importantly, the post-sanitization distribution collapses into a single distribution within the program state, indicating that all previously erased cells have been successfully programmed. This confirms the physical effectiveness of the overwrite sanitization process.

5.2.2 Evaluation of Post-Sanitization Disturbance on a Valid Page V_{th} Distribution. Figure 5(b) illustrates the impact of the sanitization process on a valid page that shares the same WL as the invalid pages within a flash block. Specifically, the Mona Lisa image is written on a flash page in the last SB (SB-11) of the targeted flash memory layer. The corresponding V_{th} distribution of the programmed flash memory page is shown in black. Initially, a sufficient voltage margin exists between erase and program states, ensuring reliable reads with zero RBER.

As overwrite sanitization operations are performed on pages in other SBs (from SB-0 through SB-10), the V_{th} distribution of the valid page in SB-11 evolves. The plot reveals a notable upward shift in the erase distribution, while the program distribution remains relatively unchanged. This shift reduces the voltage margin between two states, causing increased overlap of distributions and raising the risk of uncorrectable bit errors, thereby compromising the reliability of data stored in the affected valid pages. Note that testing across multiple FG chips of the same part number consistently revealed significant disturbances following sanitization, rendering the implementation of page-overwrite sanitization impractical for this technology.

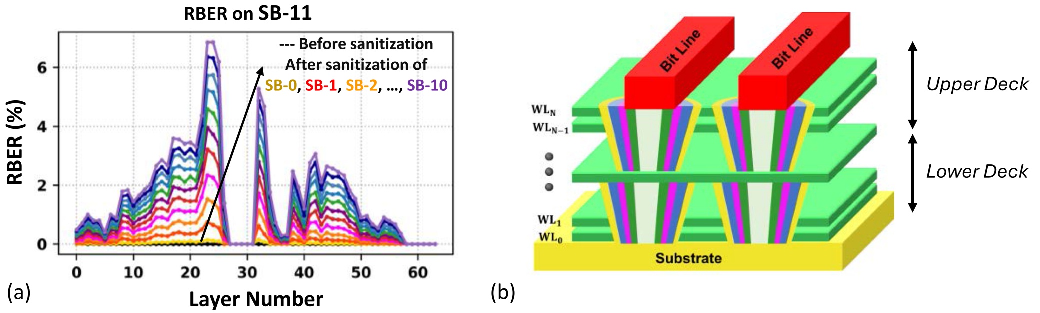

Fig. 6. (a) Effects of sanitization on the RBER of valid pages across different layers in the last SB (SB-11). Different colors represent cumulative disturbance caused by the number of sanitized SBs. (b) A cartoon illustrating dual-deck technology.

5.2.3 *Evaluation of Post-Sanitization Disturbance on Valid Page RBER.* Figure 5(c) illustrates the cumulative increase in RBER of valid pages as the number of sanitized pages within a given vertical layer increase. RBER is closely tied to the cell's V_{th} distribution. During read operations, V_{ref} is used to determine the state of a flash cell. A bit error occurs when a cell's V_{th} shifts across V_{ref}, leading to incorrect readout. As shown in Figure 5(b), the erase-state V_{th} distribution shifts upward due to repeated sanitization. This results in a larger number of erase state cells with V_{th} exceeding V_{ref}, causing $1 \rightarrow 0$ bit errors. The total number of such cells directly contributes to the measured RBER.

Figure 5(c) quantifies this effect, showing that sanitizing a single page within a layer causes the RBER of adjacent valid pages to exceed 0.1%. This surpasses the correction capability of standard ECC engines, resulting in an uncorrectable bit error rate (UBER) [23]. While NAND vendors typically mitigate the effects of V_{th} distribution shifts through read-retry mechanisms [17], by adjusting V_{ref} to optimize read accuracy, this technique becomes ineffective when two distributions begin to overlap significantly. Ideally, V_{ref} is positioned at the crossover point between the erase and program distributions, but this crossover itself shifts with increasing sanitization. Beyond a certain point, even the optimal V_{ref} adjustment cannot prevent UBER.

5.2.4 *Evaluation of Layer-Dependent Disturbance.* Figure 6(a) illustrates how disturbance effects caused by the sanitization process vary by layer within the 3D stack. The analysis focuses on the valid flash pages within the last SB (SB-11) and tracks cumulative disturbances caused by successive sanitization of other SBs. Initially, before the sanitization process begins, all pages in the SLC configuration exhibit zero RBER. However, even after the sanitization of the first SB (SB-0), a non-zero RBER appears in the valid page of SB-11. As more SBs are sanitized, RBER continues to rise. After the sanitization of the second and third SBs, the RBER may exceed the ECC correction threshold, leading to uncorrectable errors. This highlights that, despite SLCs typically having wider voltage margins, 3D NAND is still highly vulnerable to overwrite-induced disturbance.

The layer-dependent RBER trends in Figure 6(a) reveal that middle layers in the 3D NAND stack are more susceptible to disturbance than edge layers. This vulnerability is attributed to the pre-charge operation, a process typically performed before programming to minimize program disturbances on erased cells. Pre-charge voltages are typically applied through the BLs (top) and the substrate (bottom). Edge layers, being closer to both, benefit more from pre-charge conditions that reduce their susceptibility to disturbance during overwrite operations. In contrast, middle layers receive attenuated pre-charge. This is especially the case in pre-programmed blocks, where

Table 2. Summary of Median RBER Impact Due to Overwrite Sanitization

	SLC			**TLC**								
Samples	**Before San.**	**After Normal San.**	**After PULSE San.**	**Before Sanitization**			**After Normal Sanitization**			**After PULSE Sanitization**		
				LSB	**CSB**	**MSB**	**LSB**	**CSB**	**MSB**	**LSB**	**CSB**	**MSB**
64-layer FG	0%	0.93%	0%	0.01%	0.01%	0.02%	1.29%	1 2.88%	1 2.65%	0%	0.06%	0.57%
64-layer CT	0%	0%	0%	0.06%	0.04%	0.10%	5.09%	1.61 %	0.07%	0.79%	0.02%	0.03%
176- layer CT	0%	0%	0%	-	-	-	-	-	-	-	-	-

the programmed cells in the edge layers prevent the voltage propagation to the middle layers. This weakened pre-charge operation leaves the middle layers more vulnerable to programming disturbances. Interestingly, this weakening effect is absent when write operations are performed on an erased flash memory block, as the erased state allows pre-charge voltage to propagate freely into the middle layers. To address this issue, 3D NAND manufacturers recommend adhering to a proper page programming sequence, starting with the bottom-layer pages and progressing sequentially to the middle and top-layer pages. This practice ensures more uniform pre-charge conditions across the stack, thereby minimizing program disturbances.

Figure 6(a) also reveals a distinct discontinuity in RBER around layer 32, corresponding to the boundary between two fabrication tiers (or decks). This behavior stems from the two-tier or dual-deck (see Figure 6(b)) fabrication process used in NAND memory to increase layer count [12, 13, 15]. For example, the chip under test contains a total of 64 layers, with the first 32 layers forming the bottom tier (or the lower deck) and the remaining 32 layers constituting the top tier (or the upper deck). This discontinuity in RBER reflects process variation and structural asymmetry between the two decks, underscoring how fabrication techniques influence disturbance behavior across the flash memory stack.

5.3 Evaluation of Sanitization in SLC CT 3D NAND

5.3.1 Post-Sanitization Disturbance on Valid Page RBER. To further assess the feasibility of overwrite sanitization, we evaluate multiple 3D NAND chips with CT architecture from two major manufacturers. Interestingly, our findings reveal that overwrite sanitization can be successfully implemented on CT chips, without affecting the RBER of valid pages. Table 2 summarizes these results, demonstrating that CT 3D NAND chips maintain zero RBER on valid flash memory pages even under worst-case sanitization scenarios (Step-3 in Figure 4(b)). Simultaneously, the invalid target pages were confirmed to convert to an all-zero state after sanitization, ensuring complete data sanitization. These results suggest that, while overwrite sanitization poses challenges for certain 3D NAND chips (e.g., 64-layer FG SLC chips), it is a viable solution for CT-based 3D NAND chips. This differentiation underscores the critical role of 3D NAND architecture in determining the suitability of data sanitization techniques.

5.3.2 Post-Sanitization Disturbance on Vth Distribution. Figure 7(a)–(b) illustrates the impact of sanitization operations on the V_{th} distribution for the erase and program states of an invalid and a valid flash memory page located in the last SB (SB-5, as the test chip contains 6 SBs total), respectively. The plots show how these distributions evolve as overwrite sanitization is successively applied to sub-blocks SB-0 through SB-4. The results reveal that while the erase state distributions shift upward with each successive sanitization operation, a significant voltage margin persists

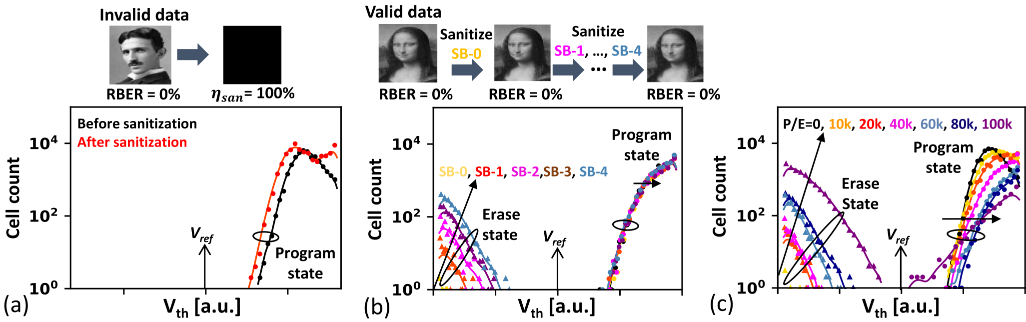

Fig. 7. Cell V_{th} distribution as a function of successive sanitization of (a) invalid page, (b) valid page, and (c) **program/erase** (**P/E**) cycle count.

between the program and erase distributions, even under the worst-case sanitization scenario. This substantial voltage margin ensures that no overlap occurs, thereby ensuring zero RBER in the valid pages. These findings suggest that CT flash memory employs a more robust pre-charge voltage scheme, effectively mitigating the impact of overwrite-induced disturbances.

Although CT chips exhibited zero RBER in our tests, the underlying disturbance mechanisms caused by the overwrite operations are believed to be similar to those observed in FG-based architectures. However, the zero RBER in CT flash memory after sanitization can be attributed to the following factors. First, the CT flash memory chip may implement a more effective pre-charge voltage propagation scheme than the FG flash chip. Enhanced pre-charge efficiency reduces program disturbances by ensuring better charge equalization, making CT flash memory more resilient to disturbances introduced during overwrite sanitization. Second, CT flash memory may possess a wider voltage margin between the erase and program state distributions, providing a greater tolerance to disturbances. Due to the limited measurement range of the Read-offset command, the exact voltage margin of the erase V_{th} distribution immediately after the program operation could not be measured, leaving this hypothesis unverified.

5.3.3 Evaluation of Disturbance on P/E Cycled Block. Figure 7(c) illustrates the effect of P/E cycling on post-sanitization disturbances in valid flash memory pages of CT-based 3D NAND memory. The measurements were taken from the same flash memory block under identical sanitization conditions, but with varying P/E cycle counts. The results indicate that disturbance severity increases with higher P/E cycling, indicating that wear-out degrades the flash memory block's ability to withstand overwrite operations. This behavior can be explained by P/E-induced degradation that causes gate oxide breakdown, which, in turn, introduces additional leakage paths within the flash memory array. These leakage paths reduce the efficiency of the pre-charge operation, as a significant portion of the pre-charge voltage dissipates through these leakage pathways. Consequently, diminished pre-charge efficiency leads to increased disturbances in P/E-cycled blocks during sanitization. Although the overwrite-based sanitization technique increases disturbances V_{th} distribution, the trend observed in Figure 7(c) suggests that the technique remains applicable even under high P/E cycling conditions in SLC-based 3D CT NAND flash memory.

5.4 Evaluation of Sanitization in TLC CT/FG 3D NAND

Previous studies have primarily evaluated overwrite sanitization in the context of SLC flash memory. However, the concept can be extended to TLC flash memory as illustrated in Figure 1(e). Here we present the results of the first experimental characterization of overwrite sanitization in TLC 3D NAND memory. In TLC devices, each WL stores data across three different logical pages,

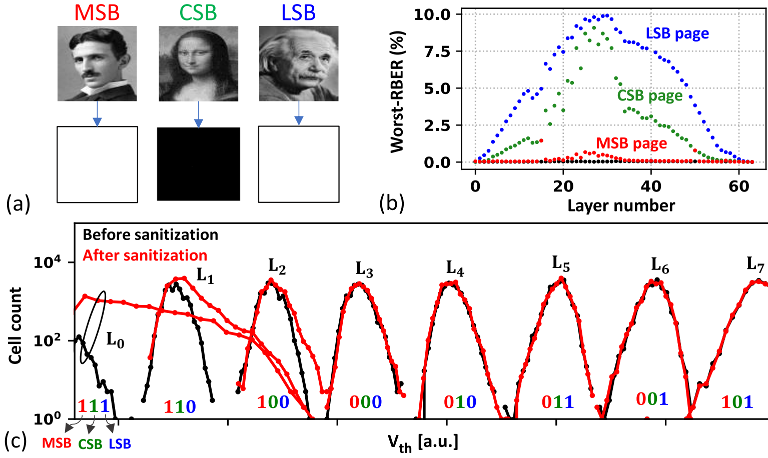

Fig. 8. (a) Illustration of sanitization operation in TLC flash, where all three logical pages are sanitized together. (b) Post-sanitization disturbances on valid flash pages across different vertical layers of CT 3D NAND flash. (c) Sanitization impact on V_{th} distribution.

namely LSB, MSB, and CSB pages. Sanitizing a single WL thus removes data from all three pages simultaneously. This is achieved by reprogramming all bits to the highest program level (i.e., L_7 state). Depending on the encoding scheme, the overwritten logical pages will transform into either an all-zero or all-one page following the sanitization process.

5.4.1 Evaluation of Disturbance on Different Logical Pages. Figure 8(a) illustrates the results of overwrite sanitization applied to a CT 3D NAND chip. Images of Einstein, Mona Lisa, and Tesla were written on LSB, CSB, and MSB pages, respectively. After sanitization, these pages transform into uniform black or white patterns. For a chip using "101" as the Gray code representation of the highest program state, the LSB and MSB pages become solid white, while CSB pages become solid black. Thus, the sanitization operation completely removes data from the invalid pages. However, overwrite sanitization also introduces program disturbance on valid pages located in adjacent SBs sharing the same physical layer. To evaluate this, we perform overwrite sanitization on all pages in SB-0 and measure disturbance on valid pages of the adjacent SBs. Figure 8(b) shows the RBER of valid logical pages in the neighboring SB across all 64 layers. The RBERs exceed the correction capability of standard ECC in most cases, resulting in unrecoverable errors. Among the three logical pages, LSB pages show the highest susceptibility to disturbances, while MSB pages are the least affected.

The underlying cause of these disturbances is illustrated in Figure 8(c), which shows the evolution of the V_{th} distribution across TLC states. Similar to SLC flash memory, the erase state (i.e., L_0) distribution shifts significantly upward, crossing the read reference voltage after sanitization. Since the L_0 state is encoded as "111" and the next program state L_1 as "110," this upward shift in the erase state distribution critically impacts the RBER of LSB pages with $1 \longrightarrow 0$ bit-flips, leading to higher error rates in LSB pages. Figure 8(c) also demonstrates that overwrite sanitization causes distortion to L_1 and L_2 state distributions, leading to increased RBERs of the corresponding CSB and MSB pages. Interestingly, the higher program states (e.g., L_3 and higher) remain relatively unaffected. These results suggest that lower V_{th} states are more vulnerable to program disturbances caused by overwrite sanitization. Such effects could potentially be mitigated by increasing precharge voltage during the overwrite process. If NAND manufacturers were to provide a specialized

overwrite command with enhanced pre-charge capabilities, the severity of such disturbances could be reduced.

5.4.2 Evaluation of Layer-Dependent Disturbance. Another noteworthy trend, visible in Figure 8(b), is the layer-dependent RBER pattern: valid pages located in middle layers are more susceptible to sanitization disturbances. This behavior mirrors the trend observed earlier in SLC FG 3D NAND devices, as described in Figure 6(a). We attribute this to the same issue of inefficient pre-charge voltage propagation into the middle layers due to the inherent architecture of 3D NAND technology. Consequently, the layer dependence of sanitization disturbances appears to be a universal characteristic across different 3D NAND architectures, affecting both FG and CT devices.

5.4.3 Multi-Chip Evaluation. To generalize our findings, we performed overwrite sanitization experiments on multiple TLC 3D NAND chips from three major manufacturers, including both FG and CT variants. In each test, only pages in the first SB were sanitized, and the RBERs of valid pages from the last SB were measured. This setup represents the minimum disturbance scenario per flash memory layer. A summary of these results is presented in Table 2, which shows the median RBERs before and after overwrite sanitization for a range of tested chips. Despite this conservative approach, all tested chips exhibited significantly elevated sanitization-induced disturbances on valid flash memory pages. These disturbances consistently surpassed the error correction capability of standard ECC, making direct implementation of overwrite sanitization impractical for TLC storage. Note that the evaluation of TLC-mode sanitization on the 176-layer CT NAND chip cannot be properly performed once all pages within a block are programmed (i.e., the block is closed).

5.5 Key Observations/insights from Experimental Evaluation

In summary, our experimental evaluation yields the following key observations and insights:

- **Reliability impact on CT vs. FG**: We find that FG 3D NAND chips are more vulnerable to overwrite-induced disturbances compared to CT chips. In FG devices, post-sanitization corruption of valid data is observed in both SLC and TLC. In contrast, CT flash memory chips demonstrate robustness in SLC mode but are found vulnerable in TLC mode. We believe that the higher sensitivity of the FG chips to sanitization-induced disturbance is mainly due to their unique array structure and pre-charge voltage conditions.
- **Impact on V_{th} distribution for SLC and TLC storage:** Post-sanitization disturbances primarily cause an upward shift in the erase-state V_{th} distribution in SLC flash memory, causing $1 \rightarrow 0$ bit flips. In the case of TLC flash memory, the lower states (L_0, L_1, and L_2) experience a voltage upshift after sanitization, while the higher V_{th} states are relatively unaffected. These effects will cause variable RBER increase on logical pages based on the data encoding scheme.
- **Layer-dependent vulnerability:** Pages located in the middle layers in the 3D NAND stack exhibit significantly higher vulnerability to post-sanitization disturbances than those located at the edges due to inefficient pre-charge voltage. Thus, the number of sanitization operations needs to be restricted in the middle layers to minimize the risk of data corruption.
- **Increased post-sanitization disturbances in P/E cycled blocks:** P/E cycled flash memory blocks are more susceptible to post-sanitization disturbances, which impose further constraints on overwrite sanitization on worn-out blocks. The storage controller should implement an adaptive scheme for heavily cycled flash memory blocks to minimize the impacts of sanitization and reduce the risk of data corruption. For example, the number of overwrite sanitization operations can be lowered on higher P/E cycled blocks.

These findings highlight the design-space metrics for implementing overwrite sanitization in 3D NAND flash memory. Successful deployment requires a thorough evaluation of device-specific characteristics and innovative design strategies to mitigate disturbances while ensuring data integrity.

6 PULSE: Partial Update for Low-Disturbance Sanitization Engine

To mitigate the disturbance caused by overwrite sanitization, we propose PULSE, a Partial Update for Low-disturbance Sanitization Engine. PULSE is a page-overwrite-based technique that balances the trade-off between sanitization efficiency on invalid target pages and disturbance minimization on valid pages. The sanitization efficiency of invalid target pages is defined in Section 5.1 as Eq. (1). It is evaluated by comparing the read-out content of a sanitized (invalid) page with a solid data pattern, which can be either all-zero or all-one, depending on the logical page type. For example, a 100% sanitization efficiency in SLC storage indicates that the invalid page data has been fully converted into an all-zero data pattern, rendering it logically irrecoverable. However, it is important to note that even partial sanitization (i.e., efficiency $< 100\%$) can still achieve logical irrecoverability, while inducing significantly less disturbance on nearby valid pages. The disturbance's impact on the valid pages is measured by $RBER^{valid}$. PULSE offers a framework to systematically balance these two competing metrics, $RBER^{valid}$ and η_{san}^{inval}, to achieve practical, low-disturbance sanitization for 3D NAND flash memory.

6.1 Implementation Algorithm of PULSE in COTS NAND Chips

The algorithm for implementing PULSE sanitization is presented in Algorithm 1 and illustrated in Figure 9. Similar to traditional overwrite sanitization, PULSE involves overwriting the target page with a solid data pattern (e.g., all-zero for SLC pages). However, the key distinction of PULSE lies in its premature termination of the overwrite process, achieved by issuing a RESET command after the program operation. The delay between the start of the overwrite and the RESET command, referred to as the partial program time (t_{pp}), is a tunable parameter that controls the trade-off between sanitization efficiency and program disturbance. The following algorithm can be used to fine-tune t_{pp} based on the characteristics of the specific NAND flash device. The initial value of the t_{pp} can be set as a fraction of the nominal page program time (t_{prog}) as $t_{pp} = \alpha t_{prog}$, where α is a design parameter with a typical value ≈ 0.5. If this initial t_{pp} does not meet the required sanitization efficiency, the overwrite process can be repeated with a longer t_{pp}, as illustrated in Figure 9. Two additional design parameters, β and γ, define the target thresholds: β represents the minimum acceptable sanitization efficiency for the invalid page (typically 80–90%), and γ denotes

ALGORITHM 1: PULSE sanitization

Initialize:

A selected page, where data has become invalid;
Estimate partial program time ($t_{pp} = \alpha t_{prog}$);
Initialize page buffers with solid data pattern;

Perform:

Sanitize invalid page based on time delay;

1. Issue NAND page program command (0x10);
2. Apply time delay (t_{pp});
3. Issue NAND RESET command (0xFF);
4. Issue page READ command to evaluate η_{san}^{inval} and $RBER^{val}$;
5. If $\eta_{san}^{inval} < \beta$ and RBER $<\gamma$ then increase t_{pp} and repeat 1 to 5
6. Else stop sanitization

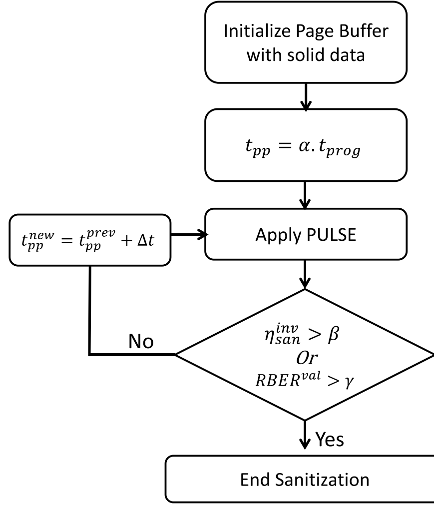

Fig. 9. Algorithm for PULSE implementation and t_{pp} evaluation.

the maximum tolerable RBER on valid pages (typically 0.1–0.5%). If PULSE is implemented through FTL, these parameters (α, β, and γ) needs to be pre-defined in the FTL firmware based on characterization results for the given storage technology.

6.2 Mechanism Behind PULSE: Sanitization Efficiency and RBER Trade-offs

Figure 10(a) illustrates the inherent trade-off between η_{san}^{inval} and $RBER^{val}$ in the PULSE sanitization approach, as demonstrated using a 3D SLC NAND device. The key tunable design parameter in PULSE is the t_{pp}, which impacts both η_{san}^{inval} and $RBER^{val}$. To illustrate this trade-off, we write a Mona Lisa image on a valid page and a Tesla image on a page designated for sanitization. The latter is then sanitized using an all-zero data pattern. At shorter t_{pp} durations, the overwrite process is prematurely terminated, leaving parts of the Tesla image visible. The resulting sanitization efficiency is poor ($\eta_{san}^{inval} < 80\%$) when compared to a complete black (all-zero) image. However, shorter t_{pp} values minimize disturbance on the valid page, keeping the Mona Lisa image intact with its RBER near zero and no visible corruption.

Conversely, as t_{pp} increases, the invalid data progressively transitions into a completely black image, reflecting improved sanitization efficiency. However, this improvement comes at the cost of higher disturbance on the valid page, resulting in an increased RBER. The plot in Figure 10(a) highlights the optimization window around $t_{pp} \approx 550$ μs, where η_{san}^{inval} reaches 98% and $RBER^{val}$ remains as low as 0.002%. This point represents a balanced trade-off, offering an adequate level of data sanitization with minimal disturbance to valid data. Note that normal sanitization results in $t_{pp} \approx 810$ μs, achieving $\eta_{san}^{inval} = 99.9\%$ but increasing $RBER^{val}$ to 0.1%. For a practical sanitization purpose, we can choose $\eta_{san} = 90\%$ corresponding to $t_{pp} \approx 330$ μs, which will cause even lower impact on RBER. Thus, PULSE introduces a flexible and practical approach to mitigating overwrite-induced disturbances in 3D NAND flash.

The physical mechanism behind PULSE's reduced disturbance is further examined in Figure 10(b)–(c) through the cell V_{th} distribution. Figure 10(b) presents the V_{th} distribution of an invalid page before and after sanitization, while Figure 10(c) shows the V_{th} distribution of a valid page that shares the same WL as the invalid page. Before sanitization, two distinct V_{th} distributions are observed, corresponding to the erase and program states. Although the erase-state distribution

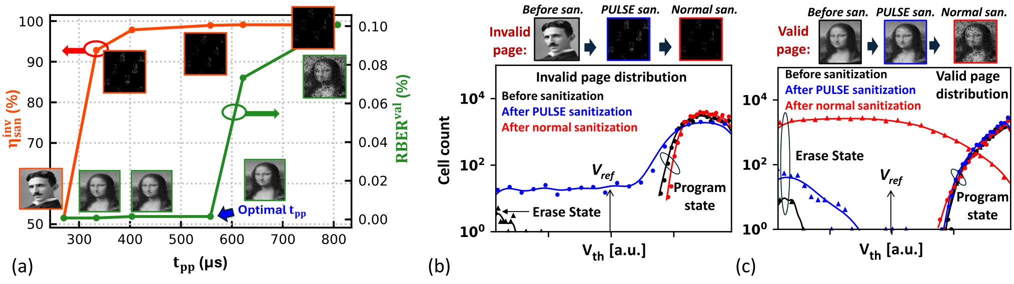

Fig. 10. (a) Illustration of sanitization efficiency and RBER trade-off in PULSE sanitization as a function of t_{pp}. Cell V_{th} distribution on (b) invalid page and (c) valid page after PULSE vs. normal sanitization.

is only partially captured due to measurement limitations, its tail remains visible. After normal sanitization, the V_{th} of the originally erased cells shifts and merges with that of programmed cells, effectively converting all data to logical "0" and achieving a sanitization efficiency close to 100%. In contrast, PULSE sanitization preserves some cells in the erase state, resulting in a wider lower tail of the program distribution. However, the advantage of PULSE is evident in the V_{th} distribution of valid data, as shown in Figure 10(c). With normal sanitization, the erase-state distribution of the valid page shifts upward, encroaching into the program-state and causing overlap between distributions, which increases the RBER. However, PULSE sanitization minimizes this upward shift of the erase-state distribution, maintaining a sufficient V_{th} margin between the states and thereby keeping the RBER of valid pages near zero.

6.3 Evaluation of PULSE on SLC NAND

While the mechanism behind PULSE sanitization was explained in the previous section, Figure 11 presents a detailed layer-dependent evaluation of PULSE on FG-type SLC 3D NAND. The FG-type is chosen for this evaluation because it exhibits significant RBER on valid pages after standard sanitization operations. In contrast, CT-type SLC 3D NAND exhibits strong immunity to such disturbances, rendering PULSE unnecessary for that class of devices.

Figure 11(a) shows the RBER observed on valid pages across different storage layers under the worst-case sanitization conditions. Here, the "worst-case" refers to a scenario where all but one page in a layer is sanitized, and the RBER is measured on the last valid page. For example, the tested FG SLC chip contains 12 SBs per layer. Thus, 11 pages in each layer are sanitized sequentially, and the cumulative RBER is measured on the last remaining page. Different colors in Figure 11(a) correspond to varying target η_{san}, each achieved by adjusting the t_{pp}, as indicated in the inset. A longer t_{pp} leads to higher η_{san}, but also greater RBER on the valid page. The results show that the RBER impact can be significantly reduced by selecting a lower η_{san} for invalid pages. For instance, maintaining η_{san} below 96% keeps RBER under 0.1% across all layers, which is well within the correction capability of standard ECC. Since the middle layers are more susceptible to disturbance, adopting a layer-dependent η_{san} strategy can optimize both sanitization efficiency and RBER impact. In this chip, for example, high η_{san}(∼99%) can be applied to the top and bottom 10 layers, while slightly reduced efficiency (∼96%) in the middle layers ensures effective sanitization without triggering ECC failures.

NAND flash storage has finite endurance, typically quantified by the number of P/E cycles a block can undergo, denoted as N_{PE}. Figure 11(b) illustrates a strategy for adapting PULSE implementation based on the P/E cycle condition of an SLC block. To achieve the same target η_{san}, a fresh block requires a slightly longer t_{pp} compared to a block that has undergone multiple P/E cycles.

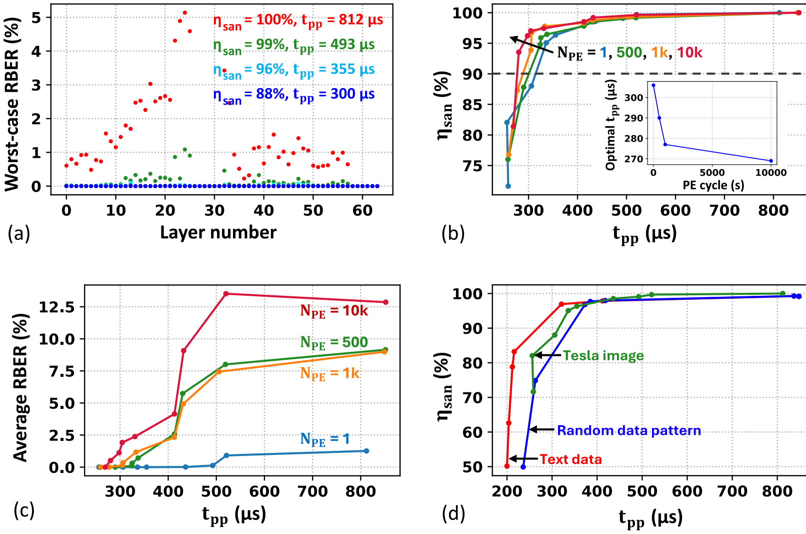

Fig. 11. (a) RBER impact on valid pages across different layers after sanitization in SLC FG storage. (b) The η_{san} for different P/E cycled blocks as a function of t_{pp}, with optimal t_{pp} vs. PE cycle (s) provided. (c) RBER impact of PULSE on different PE cycled blocks. (d) The η_{san} for different types of data files as a function of t_{pp}.

The inset in Figure 11(b) shows how the required t_{pp} for achieving $\eta_{\text{san}} = 90\%$ decreases as N_{PE} increases. This trend arises because the page program time in NAND flash tends to slightly decrease with P/E cycling due to effects such as oxide trapping. Consequently, t_{pp} must be dynamically adjusted based on the P/E cycle condition of the SLC block to ensure the target sanitization efficiency. Figure 11(c) shows the RBER impact of PULSE sanitization on different P/E cycled blocks. Fresh blocks experience significantly lower RBER impact compared to the P/E cycled blocks. In general, RBER increases with longer t_{pp}. The results in Figure 11(b) and Figure 11(c) indicate that the choice of t_{pp} is critical to optimize the trade-offs between η_{san} and RBER.

Although image data are used in this article for visualization, in the following, we evaluate PULSE on other types of data patterns. Figure 11(d) shows η_{san} as a function of t_{pp} for three different data patterns: (1) a Tesla image, represented by 8-bit grayscale pixels; (2) a text data pattern, composed of ASCII characters; and (3) a random data pattern, consisting of an equal number of 1s and 0s. Each data type is first converted to hexadecimal values and then written to flash pages. After that, we apply PULSE with different t_{pp}, and the corresponding η_{san} is recorded. The experimental results in Figure 11(d) show that the three curves representing three different data files show a very similar trend. To achieve $\eta_{san} = 90\%$, the optimal t_{pp} differs by only a few microseconds in all data types. Note that when $\eta_{san} = 90\%$, all data types become unrecognizable. Based on these results, we conclude that PULSE is effective regardless of the data pattern, confirming the robustness of this technique.

6.4 Evaluation of PULSE on TLC CT/FG NAND

In this section, we evaluate the effectiveness of the PULSE sanitization technique on 3D TLC CT and FG NAND flash memories, with the results for the 3D CT NAND flash shown in Figure 12(a)–(f). Figure 12(a) presents the impact of sanitization on the invalid target pages, while Figure 12(b) illustrates the unintended disturbance experienced by valid pages that share the same WL during the sanitization process. Images outlined in black represent data before sanitization, while

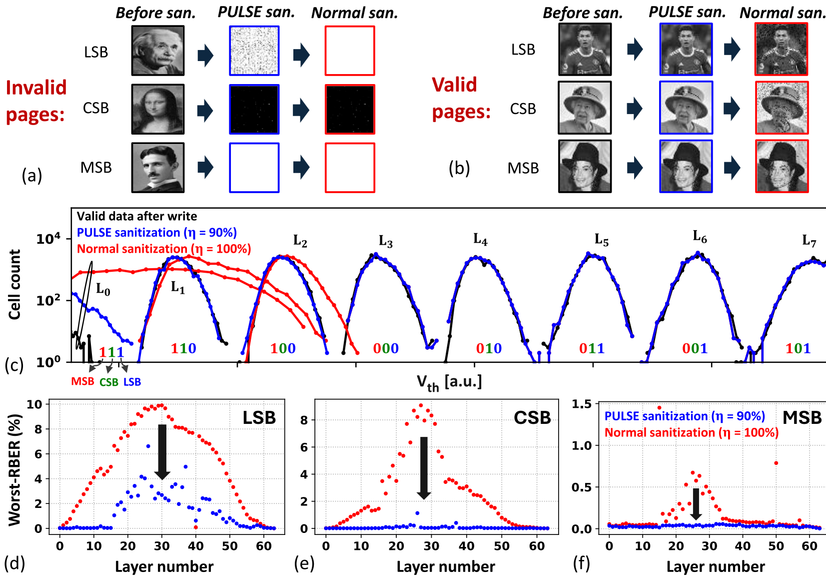

Fig. 12. Evaluation of normal and PULSE sanitization on 3D CT TLC flash memory: Images stored in (a) invalid pages and (b) valid pages before sanitization (black) and after normal (red) and PULSE (blue) sanitization. (c) Effect of the two sanitization methods on V_{th} distribution of valid data stored in 3D CT TLC flash cells. Comparison of RBER for normal and PULSE sanitization on valid flash pages across different vertical layers of 3D CT NAND flash memory: (d) LSB pages, (e) CSB pages, and (f) MSB pages.

red and blue indicate data after normal and PULSE sanitization, respectively. Given that the highest V_{th} state in CT TLC is encoded as "101", the MSB and LSB pages are converted to solid white (all-ones), and the CSB page becomes solid black (all-zeros). Normal sanitization achieves nearly 100% efficiency across all three pages, effectively erasing all traces of prior data. In contrast, PULSE sanitization achieves $\eta_{san} \approx 100\%$ for the MSB and CSB pages, but the LSB page retains partial remnants of the original data, resulting in a lower sanitization efficiency of approximately 90%.

Figure 12(b) illustrates the unintended disturbance experienced by valid pages residing on the same WL as the sanitized pages. As shown, normal sanitization introduces significant corruption to the valid data, resulting in visible degradation of image quality. Interestingly, we observe that the LSB and CSB pages exhibit greater distortion compared to the MSB page. In contrast, PULSE sanitization effectively mitigates these disturbances, preserving the integrity of all three valid pages with minimal distortion.

Figure 12(c) illustrates the origin of asymmetric disturbances on the logical valid pages by plotting the corresponding cell V_{th} distribution under three conditions: the state immediately after write (black), after normal sanitization (red), and after PULSE sanitization (blue). Based on Figure 12(c), it is evident that normal sanitization induces significant disturbance, particularly in the erase state (L_0) and the lowest two programmed states (L_1 and L_2), as indicated by the extended upper tails of the red distribution. Since MSB page data remains the same (logic-1) for all three lower V_{th} states (L_0, L_1, and L_2), it experiences minimal disturbance due to the V_{th} distortion. Only a small fraction of bits, illustrated by $L_2 \rightarrow L_3$ shift in the distribution plot, will cause errors in the MSB page. In contrast, the LSB page experiences the highest disturbance due to significant $L_0 \rightarrow L_1$ shift. The CSB page experiences a disturbance due to the $L_0 \rightarrow L_2$ and $L_1 \rightarrow L_2$ shifts. By comparison, the distribution following PULSE sanitization (blue) closely aligns

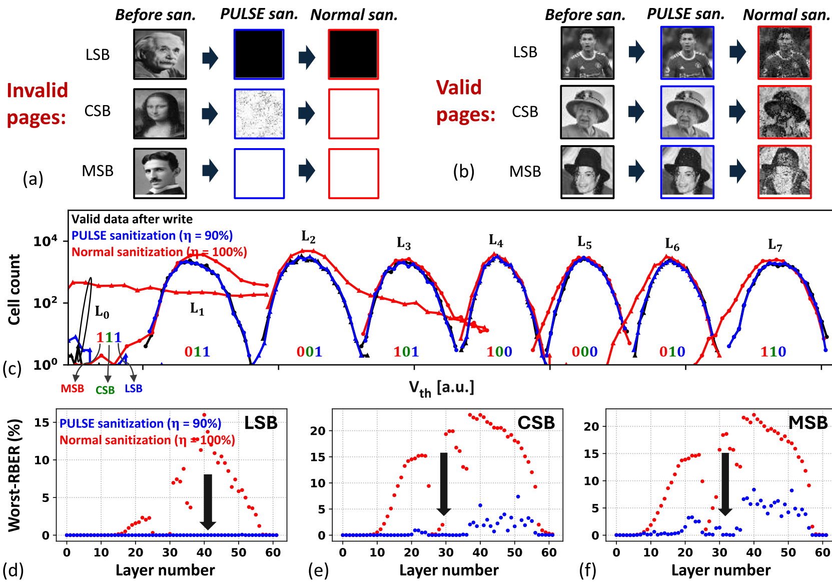

Fig. 13. Evaluation of normal and PULSE sanitization on 3D FG TLC flash memory: Images stored in (a) invalid pages and (b) valid pages before sanitization (black) and after normal (red) and PULSE (blue) sanitization. (c) Effect of the two sanitization methods on V_{th} distribution of valid data stored in 3D FG TLC flash cells. Comparison of RBER for normal and PULSE sanitization on valid flash pages across different vertical layers of 3D FG NAND flash memory: (d) LSB pages, (e) CSB pages, and (f) MSB pages.

with the original valid data distribution (black), demonstrating that the partial program approach significantly reduces the disturbance caused by normal sanitization.

Next, we evaluate the impact of PULSE sanitization on the RBER across different stacking layers. The results are presented in Figure 12(d)–(f), where Figure 12(d) corresponds to the LSB pages, Figure 12(e) to the CSB pages, and Figure 12(f) to the MSB pages. Our findings indicate that PULSE sanitization effectively reduces RBER across all three-page types. However, the middle layers continue to exhibit relatively high RBER due to inefficient pre-charge voltage, as discussed previously. Based on these results, different sanitization policies can be proposed. For example, sanitization operation on middle-layer pages can be prevented if there are valid pages on the same vertical layer. Alternatively, the number of sanitization operations on the middle layers can be restricted to a small number (e.g., one or two) to minimize RBER impact.

The effectiveness of the PULSE sanitization on FG 3D TLC NAND flash memory is evaluated, and the results are shown in Figure 13(a)–(f). Similar to CT 3D TLC NAND, the FG 3D NAND exhibits a similar trend. Figure 13(a) shows the sanitization efficiency on target (invalid) pages, while Figure 13(b) depicts disturbance to valid pages sharing the same WL. In 3D FG NAND under test, the highest programmed state (L_7) is encoded as “011” for LSB, CSB, and MSB pages, resulting in a black (all-zero) image for the LSB page and white (all-one) images for CSB and MSB pages. Similar to CT NAND, FG TLC also achieves 100% sanitization efficiency after normal sanitization, while PULSE sanitization leaves some residue traces on the invalid CSB page, as shown in Figure 13(a). However, severe data corruption is observed on CSB and MSB pages under normal sanitization, whereas PULSE causes minimal corruption in all valid pages, as shown in Figure 13(b).

Figure 13(c) depicts the V_{th} distribution of valid pages before and after PULSE sanitization. The results indicate that PULSE sanitization effectively mitigates the disturbance introduced by the

Table 3. Partial Program Time on Different NAND Flash Memory Chips

Samples	t_{pp} (η_{san} = 90%)	t_{prog} (η_{san} = 100%)
64-layer FG SLC	306 μs	849 μs
64-layer FG TLC	1.20 μs	1.79 ms
64-layer CT TLC	1.37 ms	1.95 ms

normal sanitization method, particularly for flash cells in the lower states (L_0-L_2). Figure 12(d)–(f) further evaluates the RBER across different stacking layers and shows that PULSE significantly reduces the disturbance caused by normal sanitization. Notably, the middle layers, which are more susceptible to the disturbance under normal sanitization, benefit the most.

Next, we summarize the t_{pp} required to achieve 90% of η_{san} on different NAND flash memory chips from various manufacturers in Table 3. Note that the timing values of each NAND flash memory chip are measured by probing the **ready/busy** (**RB**) pin during normal (t_{prog}) and PULSE (t_{pp}) sanitization. Typically, SLC page write requires significantly less time than TLC pages, which directly results in shorter t_{pp} for SLC configuration. The findings in this section confirm that PULSE sanitization can be successfully deployed on both CT and FG 3D NAND flash memories with both SLC and TLC configurations, resulting in a reduction in disturb-induced errors compared with normal sanitization.

6.5 Implementation Challenges and Overhead Analysis of PULSE

PULSE can be implemented on unmodified NAND chips through firmware-level support in the FTL. However, this approach introduces several challenges and performance overheads, which are discussed below:

- **Overwrite permissions**: Some NAND chips do not support overwrite operations once a flash memory block is fully programmed (i.e., the block is "closed"). As a result, PULSE cannot be implemented on such chips unless the manufacturer provides specific features or commands to enable overwrite functionality. Additionally, some NAND chips are equipped with built-in data randomizers and internal ECC engines, which can interfere with the PULSE overwrite process. However, most of the recent raw 3D NAND chips do not include these features, as NAND vendors typically offer greater flexibility to system integrators, allowing them to implement their own FTL and associated functions. Hence, PULSE can be implemented through FTL firmware on most NAND available today.
- **Precise timing control**: PULSE implementation relies on a partial overwrite operation, that is, highly sensitive to the t_{pp} and the specific behavior of the RESET command. Precisely controlling t_{pp} can be challenging for the FTL, especially during the run-time of the system. Furthermore, variations in RESET command implementations across different NAND manufacturers can introduce additional uncertainty, further complicating reliable PULSE execution. Thus, PULSE implementation will require FTL design with fine-grained timing control of NAND chips.
- **Performance overhead**: The PULSE implementation may introduce performance overheads for the FTL. Since PULSE requires multiple overwrite operations with varying partial program times, along with the determination of sanitization efficiency and RBER on valid pages, it incurs additional latency and computational overhead. However, the FTL can mitigate the impact on host-visible performance by scheduling the sanitization process in the background during the idle phase of the SSD, thereby hiding the latency from the host system.

— **RBER impact**: The most direct impact of overwrite sanitization is increased RBER on valid pages sharing the same WL as the sanitized page. While PULSE sanitization mitigates this effect, it still induces non-negligible RBER in TLC storage. Because NAND flash follows an out-of-place update strategy, overwrite operations, though supported, are rare and not optimized for latency or disturbance control. In 3D NAND, the SB architecture further amplifies vulnerability to disturbance during overwrites.

Some of the above-mentioned implementation challenges and the overhead can be mitigated with the support of NAND manufacturers. For example, an **Incremental Step Pulse Programming (ISPP)**-based programming sequence is not needed for PULSE. Instead, a single high-voltage program pulse is more appropriate for overwrite operations. NAND manufacturers can design a special command sequence to offer such a single pulse-based overwrite operation, which will minimize latency impact. In addition, the pre-charge voltage conditions can be optimized for the single pulse-based PULSE implementation, which will minimize the RBER impacts on the valid pages.

7 Implications of PULSE for Future 3D NAND SSD Design

Our findings have the following implications for the implementation of overwrite sanitization in next-generation 3D NAND SSDs:

— **Trade-off between sanitization efficiency and data integrity**: PULSE provides an effective mechanism for balancing sanitization efficiency with minimized disturbance on valid data. This makes overwrite-based sanitization feasible for 3D NAND architectures when tailored to specific applications and system requirements.

— **Enhanced PULSE implementation requires manufacturer support**: Our work demonstrates the feasibility of implementing overwrite-based sanitization, including PULSE, on commercial 3D NAND flash chips without requiring any special support from the chip manufacturers. However, even greater sanitization efficiency and lower disturbance overhead can be achieved with modest support from manufacturers. For example, vendors could introduce specialized command sequences to support shorter programming times, leveraging ISPPs, or allow for adjustable pre-charge voltage conditions during page overwrite operations. These enhancements would further reduce RBER on valid pages and improve timing precision, facilitating more reliable and efficient PULSE integration into the FTL firmware.

— **PULSE for future generations of 3D NAND**: The 3D NAND technology is poised to have more than 1,000 layers per flash memory block in the next decade. This will increase the block size of future 3D NAND chips in terms of the number of pages, causing “Big Block Issues” [1]. Thus, the implementation of PULSE will be increasingly important for the future generation of 3D NAND chips to prevent data leakage without incurring wear-out and significant performance overheads.

— **PULSE on P/E cycled block**: PULSE needs to be optimized based on the P/E cycle condition of a flash memory block. Experimental evaluation shows that optimal t_{pp} decreases with increasing P/E cycles. In addition, storage controllers may limit the number of sanitized pages per layer to ensure tolerable RBER levels for valid pages within the same layer based on underlying storage configuration, such as SLC vs. TLC.

— **Layer-specific management**: Since middle layers of the 3D stack are inherently more susceptible to post-sanitization disturbances than edge layers, storage controllers could use this insight to intelligently manage the number of sanitized pages based on layer location.

8 Conclusions

This article presents the first comprehensive experimental evaluation of overwrite-based page-level data sanitization in commercial 3D NAND flash memory, covering both SLC and TLC configurations and utilizing chips from three major vendors. Our findings show that while overwrite sanitization can achieve nearly 100% sanitization efficiency across both CT and FG SLC devices, it introduces significant reliability concerns, particularly in FG-based chips, where the RBER on adjacent valid pages can exceed ECC correction limits. TLC devices are even more vulnerable, with overwrite sanitization causing severe median RBER increases (up to ∼13% in FG and ∼5% in CT), rendering the approach impractical. Our analysis reveals that post-sanitization disturbance, caused by the upward shift of the erase threshold voltage distribution, is the primary mechanism for data corruption, with the effect being most pronounced in the middle layers of the 3D stack. To address these limitations, we propose PULSE, a Partial Update-based Low-disturbance Sanitization Engine, which significantly reduces RBER while maintaining high sanitization efficiency. PULSE achieves near-zero RBER for valid pages in SLC configurations and brings the median RBER to below 0.79% in CT and 0.57% in FG TLC flash, demonstrating its effectiveness in balancing sanitization efficiency and data integrity.

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